Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 292-293

F-4-5L

# Layout dependence of RF CMOS performance on ultra-thin Si substrate

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## 1. Introduction

3D integration has been important in order to realize both high-density system in package (SIP) and high functionality with heterogeneous integration of materials, device, and signals [1,2]. Thin chips have been effective for realizing system in package with high density [3]. Additionally, SOI substrate with around 2μm Si layer has been popular for higher breakdown device such as driver IC. We fabricated SOI structure with around 2μm Si layer by thinning bulk wafer. Thus the ultra thin Si substrate technology are useful for both the package with high density and SOI structure with around 2μm Si layer. In this paper, we discuss the MOSFET performance on ultra-thin Si substrate, comparing with thick Si substrate results.

## 2. Sample fabrication

Figure 1 and 2 show process flow of our samples. In this experiment, high-resistivity substrate (>1000Ω·cm) was used for high-Q inductor [4]. After STI process, well and channel implantation were carried out, 2.5nm gate oxynitride was formed. Co salicide process was applied to reduce parasitic resistance after gate electrode, source and drain formation. After fabrication of MOSFET on a wafer, pre-dicing of 55μm was performed in order to prevent a wafer breaking during grinding process. After setting protection tape on the front side of a wafer, Si substrate was thinned by grinding process and dry etching. The thin chip was stacked on a insulator plate and the protection tape was peeled from the chip. Figure 3 shows a TEM photograph of 0.11μm MOSFET on ultra-thin Si substrate. It was confirmed that the Si substrate thickness was 1.7μm. Figure 4 shows SIMS profile of phosphorus in Nwell. According to this profile, the junction depth of Nwell is 1.8μm and this depth was comparable with the thin Si substrate thickness. Figure 5 shows comparison of a estimated SOI substrate cost with around 2μm. The SOI wafer cost is too high while bulk wafer cost is lower and the grinding and dry etching process cost for thinner Si substrate is also low. As a result, the cost of thinned bulk substrate can be 84% lower than that of SOI wafer. This cost merit is important for telecommunication market.

## 3. Layout dependence of MOSFET performance

No degradation of the junction and gate leakage current was observed in both NMOS and PMOS in 1.7μm Si substrate case. However, MOSFET performance has larger dependence of the geometry and the layout in the ultra-thin Si substrate while the dependence in 750μm case was small. Figure 6 shows Id – Vd curves of 0.11μm NMOS for 750 and 1.7μm Si substrate. The measured MOSFET has finger length (Wf) of 5μm and finger number (Nf) of 1. In this layout, no difference of the drivability was observed in two Si substrate cases. This result shows no degradation of digital performance even when the Si substrate is 1.7μm. On the other hand, the drivability and transconductance were significantly degraded when the Nf exceeds 20. This degradation is serious problem for analog circuits because the multi finger structure has been used. We believe this degradation was caused by mechanical stress, and the degradation became larger as the length of active area increases. In order to verify this thought, we investigated analog performance in two kinds of layouts. Figure 7 shows top of view of those layouts when the finger length is 5μm. Pattern A has finger number of 40. On the other hand, pattern B consists of four MOSFETs with finger number of 10. Total gate width is 200μm in both patterns. The active area of pattern A is longer than that of pattern B for one device. Figure 8 shows drain current dependence of fT and fmax for CMOS in two kinds of layout. In pattern A, the maximum value of fT was 16% lower for NMOS and 12% lower for PMOS, comparing with 750 Si substrate case. On the other hand, fT value was improved in pattern B. The maximum value of fT was 5% lower for NMOS and 7% higher for PMOS. This is because the gm in pattern B was higher than that in pattern A. The improvement of fmax was significantly larger than that of fT because the fmax can be improved by not only higher gm but also higher substrate resistance. The maximum value of fmax was 3% higher for NMOS and 10% higher for PMOS. Additionally, the fmax – Id curve shifted to the lower current. This improvement is useful for low current consumption of RF circuits.

Figure 9 shows Id dependence of NFmin and gain for 0.11μm NMOS at 3GHz operation. Higher gain and lower NFmin were observed in 1.7μm case compared with 750μm case. The Id at 2.0dB NFmin can be reduced from 2.1mA to 0.9mA by thinning from 750 to 1.7μm Si substrate, which is 53% reduction of the current. This result shows ultra-thin chip is effective for low current consumption of CMOS LNA. Figure 10 shows explanation for the improvement of the gain and NFmin. The signal goes to the substrate by coupling between signal line and Si substrate. In order to obtain higher gain and lower NFmin, the smaller signal to Si substrate is required. The signal becomes smaller in thin Si substrate because the impedance in Si substrate increases.

## 4. Conclusions

MOSFET performance has layout dependence in ultra-thin chip with 1.7μm Si substrate. MOSFET performance of fT and fmax were degraded when the Nf was 40. However, those performances can be improved by division layout of active area, significantly.

Ultra-thin chip with 1.7μm Si substrate thickness brings about a larger reduction of NFmin. The Id at 2.0dB NFmin can be reduced from 2.1mA to 0.9mA by thinning from 750 to 1.7μm Si substrate, which is 53% reduction of the current.

## References

[1] A. Shigetou et al., Proc. ECTC 2003 pp.848-852
[2] J. Burns et al., Proc. ISSCC 2001
[3] T. Ohguro et al., Proc. VLSI Symp. 2004 pp. 220-221
[4] T. Ohguro et al., Proc. IEDM2000 pp.757 - 760

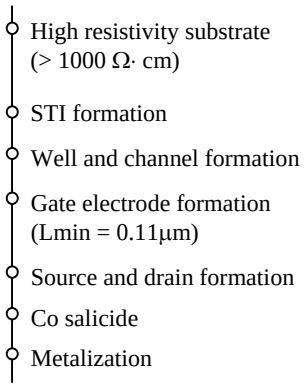



Fig.1 Process flow of CMOS. The minimum Lg was 0.11μm.

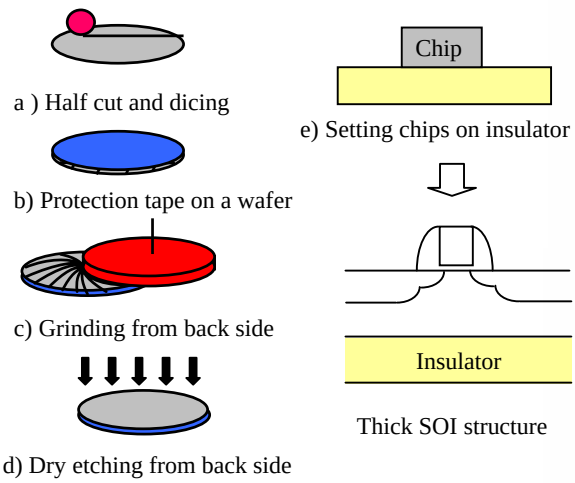



Fig.2 Process flow for fabrication of ultra thin chip by using grinding and dry etching

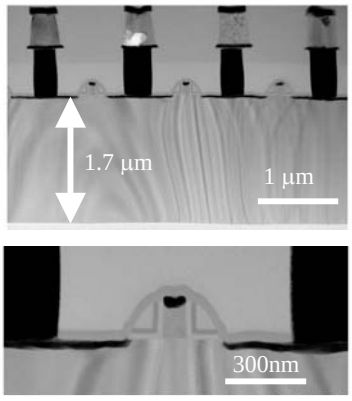



Fig.3 TEM photograph of ultra thin Si substrate.

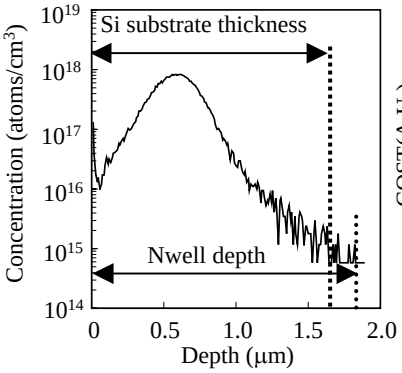



Fig. 4 SIMS profile of phosphorus in Nwell. Si substrate thickness of ultra-thin chip was comparable with the depth of Nwell

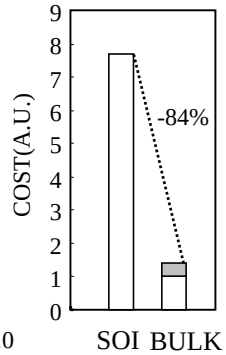



Fig. 5 Comparison of estimated SOI substrate cost with 2μm between SOI wafer and thinned bulk wafer

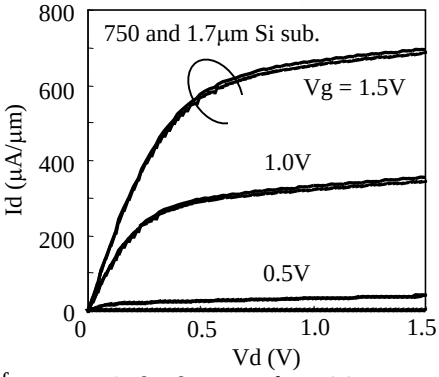



Fig.6 Id-Vd curves of NMOS as Lg = 0.11μm and Wg = 5μm for 750 and 1.7μm Si substrate thickness.

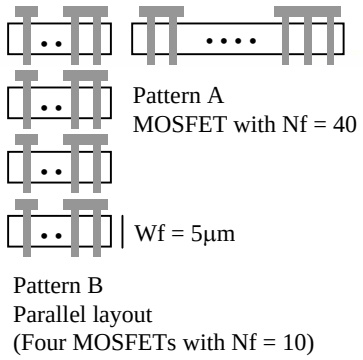
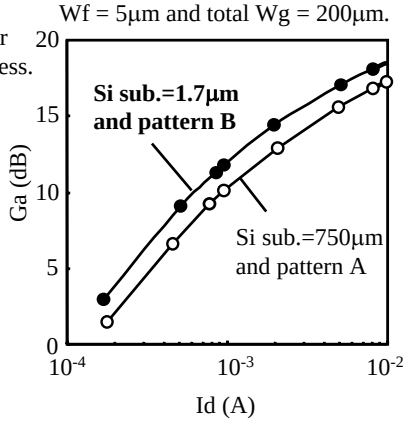



Fig.7 Two kinds of layouts for RF measurement when Lg = 0.11μm, Wf = 5μm and total Wg = 200μm.



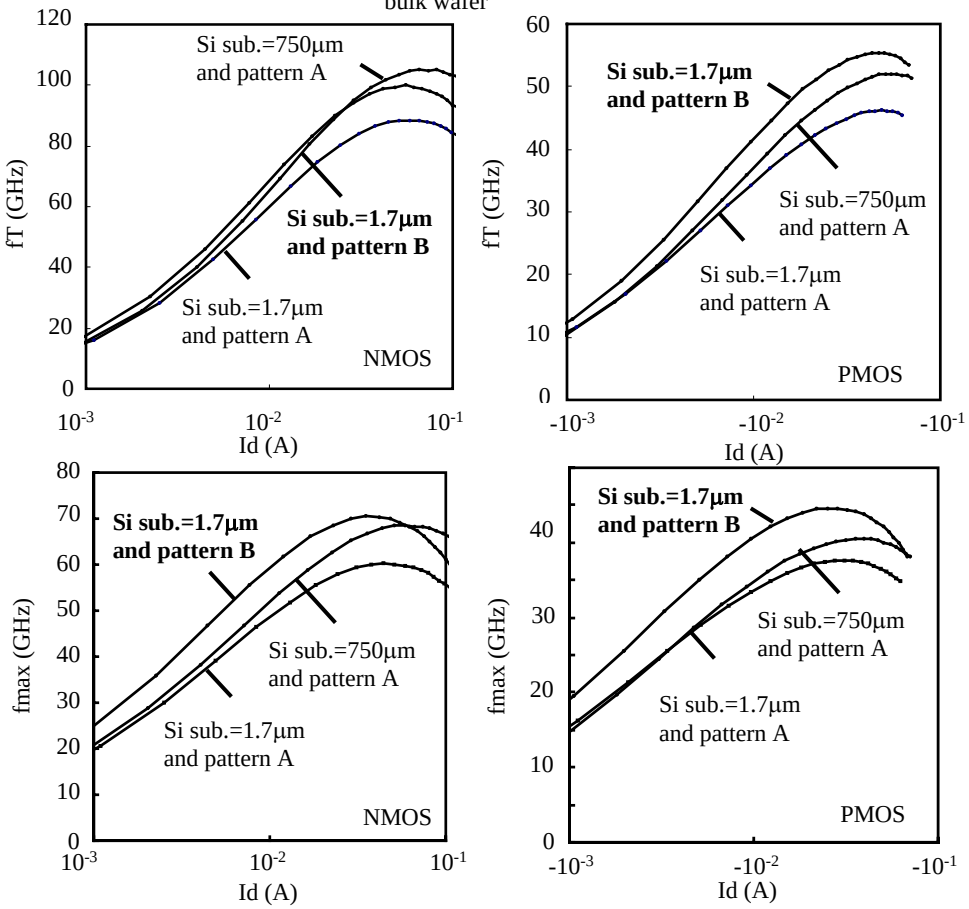




Fig. 8 Layout dependence of fT and fmax - Id curves for CMOS as Si substrate thickness is 750 and 1.7 μm. The gate length and total gate width was 0.11μm and 200μm, respectively.

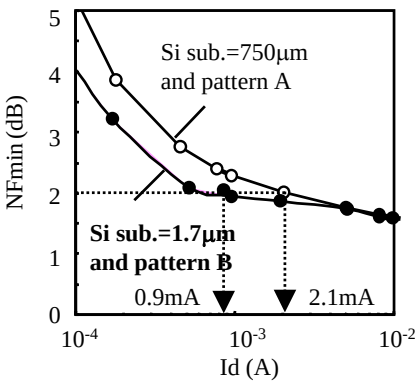



Fig.9 Drain current dependence of NFmin and gain at 3GHz operation.

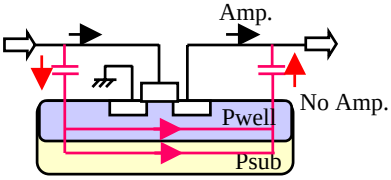



Fig.10 Explanation for the improvement of the Ga and NFmin in thinner chip