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High-Speed Transmission Circuit for Micro Network on Si ULSI

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1. Introduction

The International Technology Roadmap for Semiconductors has suggested that the delay of global interconnect on LSI is increasing in each technology node[1]. The area where the signal can be reached within one clock period is known to be only a few percents of a whole chip area. Thus, it is inevitable to break off the conventional synchronous design of the whole LSI chip. New design methods have been proposed to solve the issues relating to global interconnect delay: three-dimensional integration[2], network on chip (NoC)[3] and network in package (NiP). NoC and NiP require a special I/O drivers for long interconnects which behave as a transmission line.

This paper proposes a high-speed transmission line (TR) circuit, which can be employed for seamless interconnect in intra- and inter-chip communication shown in Fig. 1. The TR-line circuit consists of a differential transmission line, differential driver and receiver. If long interconnects are designed as a TR line, the delay of global interconnects is substantially reduced to be electromagnetic-wave speed. The TR-line interconnect on Si ULSI chip with a sufficient high crosstalk endurance has been proposed[4].

In this paper, we present measured eye-patterns of the proposed TR-line circuits that were designed and fabricated using 0.35μm and 0.18μm CMOS process technologies. The proposed TR-line interconnect with driver/receiver circuit has exhibited both high-speed signal transmission and low power consumption against the conventional RC interconnects.

2. Differential Transmission Line Structure

Figure 2 shows two-type on-chip differential transmission line (TR) structures for global interconnects; (a) co-planar and (b) diagonal pair line that has high crosstalk robustness[4]. In this paper, the co-planar type TR line of Fig. 2(a) is used for evaluation. The TR line structure is designed to have differential impedance Z_{diff} of 100Ω using 2D EM simulator (Ansoft, 2D Extractor) as shown in Fig.2. Figure 3 shows the proposed TR-line circuit. Resistances R_{in} and R_{out} are determined to achieve impedance matching, which suppress far- and near-ends reflection. The impedance matching condition is

$$2R_{out} = Z_{diff} = R_{in} .$$

We have designed and fabricated co-planer TR line and driver/receiver circuits using 0.35μm and 0.18μm CMOS technologies. Circuit parameters for 0.18μm process were as follows: (1) gate widths (W_G) of the driver nMOS differential pairs; 310μm, (2) W_G of the driver current source nMOS; 300μm. (3) W_G of the receiver nMOS and pMOS differential pairs; 20μm, (4) W_G of the current source; 200μm, and (5)V_{bias1}=0.8V and V_{bias2}=0.65V.

3. Results and Discussion

The digital oscilloscope, pulse pattern generator (PPG), RF and DC probes were used for time-domain measurement as shown in Fig. 4. Figure 5 shows a micrograph of the DUT. A pseudo random bit sequence was inputted to the DUT from PPG. Output waveforms of DUT and eye-pattern were measured by the digital oscilloscope. DC power was supplied through the DC probes to the driver/receiver circuits and output buffer inverter.

Figure 6 shows the 4Gbps eye-pattern of differential receiver output with 3-mm long TR line and 0.35μm driver/receiver circuits. The cm-long TR line itself of Fig. 2 has been confirmed to be used for over 10Gbps transmission by the authors[4]. The data transmission rate is limited by the driver and receiver circuit performance. Figure 7(a) and 7(b) show eye-patterns of 0.35μm and 0.18μm CMOS receiver circuits, respectively. The 0.18μm receiver is at least twice as fast as 0.35μm receiver. These results mean that one can expect over 10Gbps signal transmission by using sub-100nm CMOS process.

The delay time (τ_{delay}) and power consumption (***P***) of TR-line interconnect with driver/receiver circuit and the conventional RC lines with repeaters has been evaluated. The 0.18μm CMOS technology was assumed. For the differential driver/receiver circuit, input and output inverters are connected to provide rail-to-rail input and output voltages as shown in Fig. 3. Figures 8(a) and (b) show τ_{delay} and ***P*** at 4 Gbps, respectively. τ_{delay} is defined by 50%-50% voltages. τ_{delay} of differential TR-line circuit is faster than RC line for over 2.4mm-length interconnect. Furthermore, ***P*** of the differential TR-line circuit is less than that of RC line at over 7mm-long interconnect. In 65nm technology node, the number of over 1cm long interconnect is larger than 10^6, so that the proposed TR-line circuits will have a large impact on the high-performance circuit design.

4. Conclusion

This paper proposes high-speed transmission (TR) line circuit for seamless interconnect for intra-chip and inter-chip. 4 Gbps pulse signal transmission has been confirmed in 0.35μm CMOS process technology. The proposed TR-line circuit has superior characteristics against the conventional RC global interconnect at GHz signal transmission.

References
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[4] H. Ito, et. al., to be published at *IEICE Trans. Electron.* **E87-C-6** (2004).
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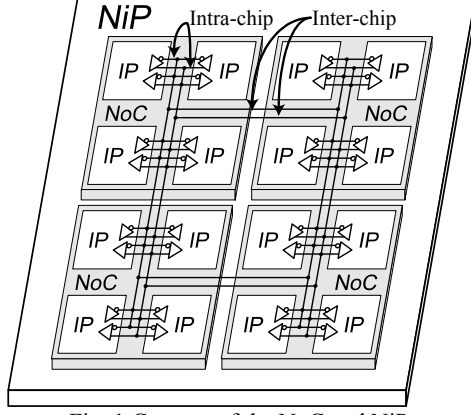[6] M. Yamashina, *et. al.*, *SSDM* (1999) 586.

Fig. 1 Concept of the NoC and NiP.

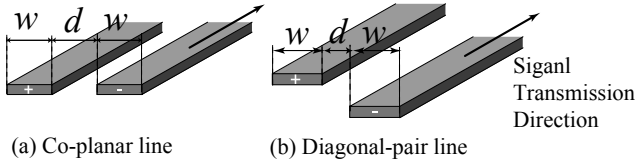(a) Co-planar line   (b) Diagonal-pair line
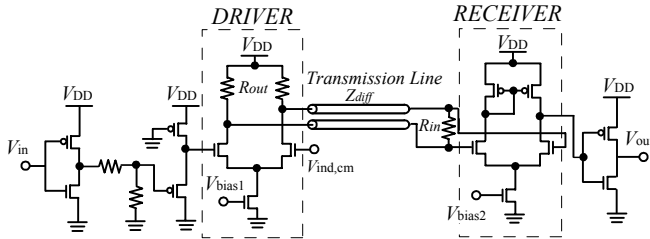
Fig. 2 Differential transmission line structure.
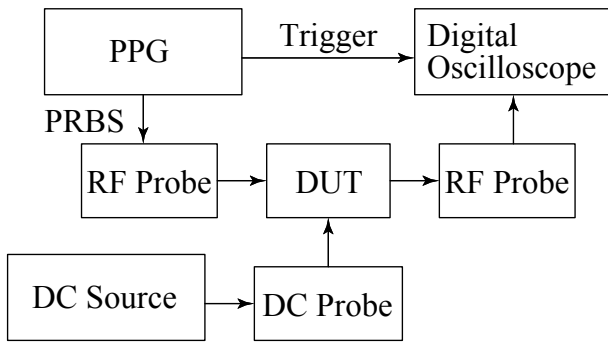

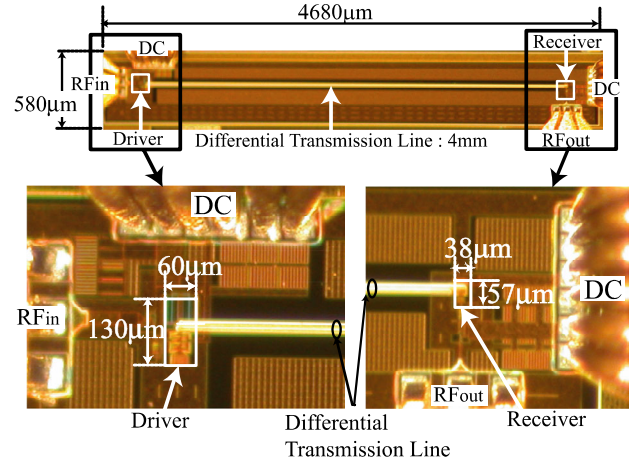Fig. 3 Driver and receiver circuits.

Fig. 4 Measurement system.

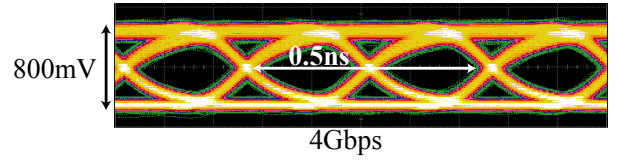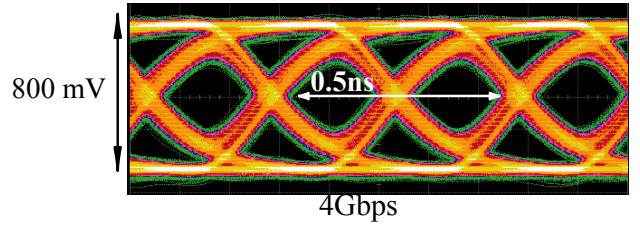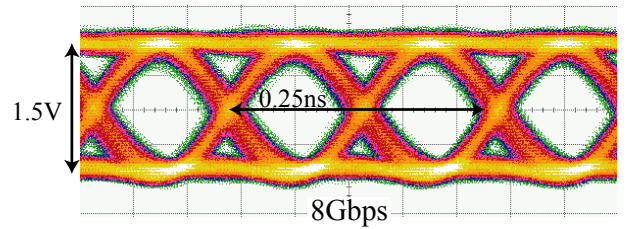Fig. 5 Micrograph of the DUT (0.18μm process).

Fig. 6   Eye pattern of differential receiver output of 0.35μm driver/receiver circuits with 3-mm long TR line.

(a) Differential receiver output. 0.35μm process.

(b) Buffer inverter output of differential receiver. 0.18μm process.

Fig.7 Eye patterns of receiver circuits.

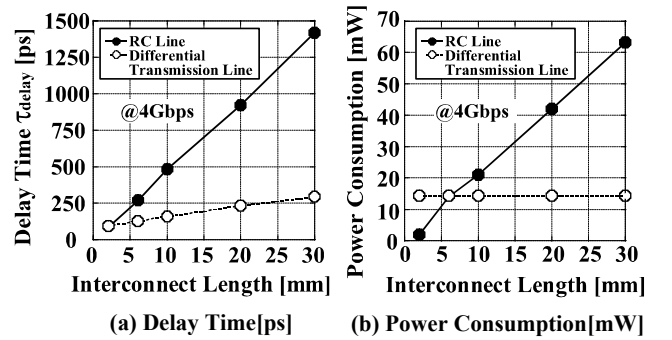(a) Delay Time[ps]   (b) Power Consumption[mW]

Fig. 8   Delaytime and power consumption at 4Gbps. 0.18μm process is assumed.