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Grain Size Dependence of Field-Effect Mobility in Pentacene-Based Thin-Film Transistors

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1. Introduction

The organic thin-film transistors (TFTs) have provided some advantages over inorganic semiconductors TFTs for applications requiring structural flexibility, low temperature processing, and low overall cost. The pentacene-based TFTs with field-effect mobility ≥ 1 cm^2/Vs have been demonstrated on the gate insulators of self-assembled monolayer treated silicon dioxide [1-6], poly-4-vinylphenol [6], and poly-(vinyl alcohol) [7]. The mobility of the pentacene TFTs are comparable to that of the amorphous silicon TFTs. In general, pentacene layer consists of dendritic grains. The pentacene transistor mobility is supposed to depend on grain size, energy barrier between grains, carrier transport in a grain, and interface between organic layer and gate insulator. It is necessary to investigate the relation between grain size and field-effect mobility of TFTs.

In this study, we have investigated influence of grain size of pentacene layer on electrical characteristics of pentacene TFTs on untreated thermal silicon dioxide. The grain size was controlled by deposition rate of the pentacene layer. The pentacene layers had average grain size from 0.98 to 6.09 μm at a deposition rate of 2.0 to 0.02 Å/s. We first demonstrated the TFT at deposition rate as low as 0.02 Å/s for the pentacene layer and obtained pentacene layer with the average grain size of 6.09 μm.

2. Experimental

Figure 1 shows a schematic cross section of the fabricated pentacene TFT. Highly *n*-type doped (100) silicon substrates with thermally grown 300-nm-thick SiO_2 were used without cleaning and surface treatment. The Si substrate serves as a gate electrode. The SiO_2 as gate insulator has a capacitance per unit area of 11.5 nF/cm^2. The root-mean-square of the SiO_2 surface roughness was about 2 Å from atomic force microscopy (AFM) measurement. Pentacene was purchased from Aldrich and was used without additional purification such as thermal gradient sublimation. A 60-nm-thick pentacene layer was thermally evaporated at a deposition rate between 0.02 and 2.0 Å/s at room temperature. The TFTs were completed by thermally evaporating a 50 nm gold layer through a shadow mask to form source and drain electrodes. The channel width and length were 2 mm and 40 μm, respectively.

The surface morphology of the deposited 60-nm-thick pentacene layer was investigated by AFM measurement. The TFTs were characterized using a KEITHLEY 4200 semiconductor characterization system in air at room temperature without capsulation. The field-effect mobility was extracted from the saturation region at a drain-source voltage V_{DS} = –100 V.

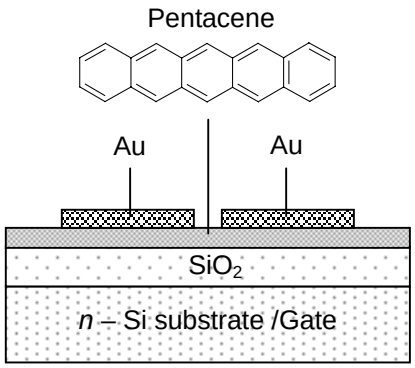

Fig. 1 Schematic cross section of a pentacene-based TFT.

3. Results

Figure 2 shows an AFM image of a 60-nm-thick pentacene layer deposited at a deposition rate of 0.02 Å/s. The pentacene layer exhibited a large dendritic grain structure with the average size of about 6 μm.

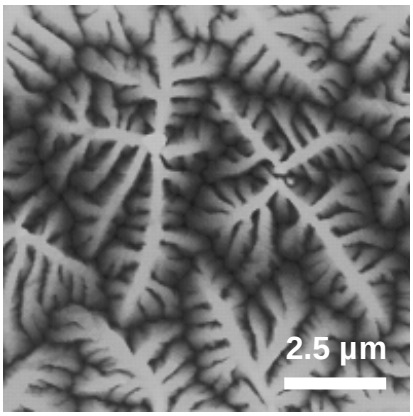

Fig. 2 An AFM image of a 60 nm thermally evaporated pentacene layer on a thermal silicon dioxide at deposition rate of 0.02 Å/s.

Figure 3(a) shows the drain current I_D versus drain-source voltage V_{DS} of a pentacene TFT at deposition rate of 0.02 Å/s with the channel width of 2 mm and the

channel length of 40 μm. The electrical characteristic of the TFT is typical behavior of a semiconductor field-effect transistor. The drain current was achieved larger than 2 mA at the V_{DS} = –100 V and gate-source voltage V_{GS} = –100 V. Figure 3(b) shows the drain current I_D versus gate-source voltage V_{GS} of the TFT. From the saturation region at the V_{DS} = –100 V, a field-effect mobility of 1.81 cm^2/Vs, an on/off current ratio of 1.90×10^7, and a threshold voltage of –6.60 V was obtained. To our knowledge, the largest mobility of the pentacene TFT as large as 0.7 cm^2/Vs has been fabricated on the untreated oxidized silicon substrate [8].

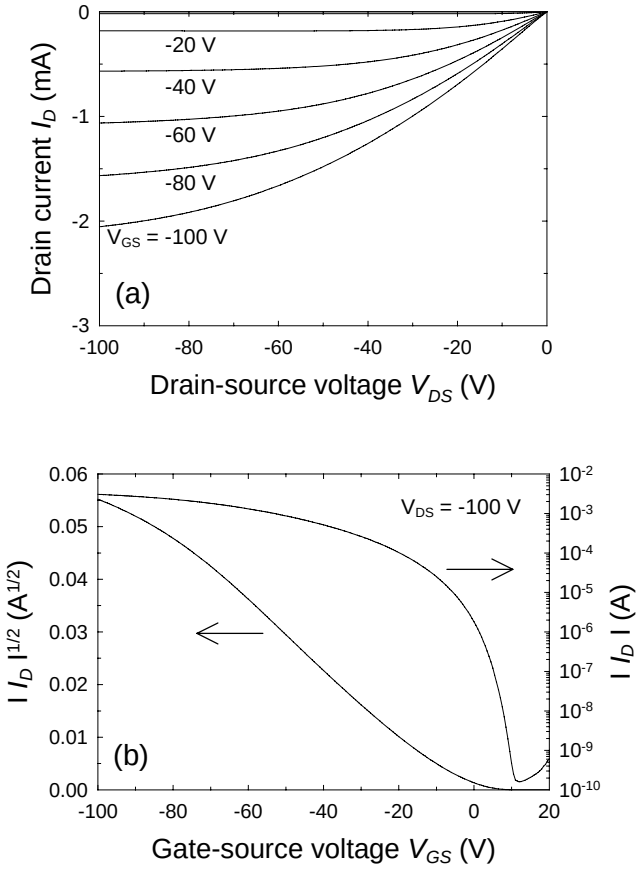

Fig. 3 Electrical characteristics of a pentacene TFT at deposition rate of 0.02 Å/s. (a) Drain current I_D versus drain-source voltage V_{DS} characteristics. (b) Drain current I_D versus gate-source voltage V_{GS} characteristics.

Table I summarizes the electrical characteristics of pentacene TFTs at various deposition rates. The average grain size increased with decreases in the deposition rate of the pentacene layer. The size of the grain was controlled by the deposition rate. More importantly, the mobility and on/off current ratio were found to increase with the grain size. The increasing mobility is probably due to the decreasing number of the grain boundaries in the channel. For the grain size of 6.09 μm, the mobility of the TFT as large as 1.81 cm^2/Vs was achieved. On the other hand, the transistor for the grain size of 0.98 μm had a mobility of 0.50 cm^2/Vs.

Table I Electrical characteristics of pentacene TFTs.

Deposition rate (Å/s)	Average grain size (μm)	Mobility (cm^2/Vs)	On/off
0.02	6.09	1.81	1.90×10^7
0.05	4.06	1.47	1.20×10^7
0.20	2.27	1.31	1.03×10^7
0.50	1.37	0.78	2.11×10^6
2.0	0.98	0.50	1.87×10^6

4. Conclusions

We have fabricated the pentacene TFTs at various deposition rates on the thermal silicon dioxide. The grain size from 0.98 to 6.09 μm was controlled by deposition rate of the pentacene layer from 2.0 to 0.02 Å/s. The field-effect mobility of the TFTs increased with the size of the grain. It was found that the grain size increased with decreasing the number of the grain boundaries in the channel of the TFTs. The TFT was fabricated at deposition rate as low as 0.02 Å/s for the pentacene layer with the grain size of about 6 μm and obtained mobility as large as 1.81 cm^2/Vs.

Acknowledgements

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