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Over-100-Gbit/s Multiplexing Operation of InP DHBT Selector IC Designed with High Collector-Current Density

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1. Introduction

High-speed ICs are indispensable components for the cost-effective construction of optical communication systems. Research on high-speed ICs has included investigations of 100-Gbit/s-class operation [1-5]. The construction of 100-Gbit/s-class digital ICs using heterojunction bipolar transistors (HBTs) requires not only a high current cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) but also a high collector-current density (J_c) [6]. However, f_T/f_{max} is generally dependent on J_c as shown in Fig. 1. In the high J_c region, f_T/f_{max} decreases as J_c increases as a result of current blocking and the Kirk effect. In order to maximize IC speed, this trade-off between f_T/f_{max} and J_c should be considered during circuit design.

In this paper, we describe the effect of increasing J_c at the expense of f_T/f_{max} on the speed of InP double heterojunction bipolar transistor (DHBT) digital ICs. To investigate this influence, we chose a selector IC as a benchmark because it is widely used as a 100-Gbit/s-class digital IC [1-5]. We designed two types of selector IC. One has a J_c at which f_T and f_{max} are almost maximum, and the other has double the J_c value at the expense of f_T/f_{max}. At an operating speed of 100 Gbit/s, the selector IC with double the J_c shows clear eye openings, while the selector IC with the J_c at which f_T/f_{max} are almost maximum does not have eye openings. Furthermore, we confirmed that the selector IC with double the J_c has eye openings at up to 145 Gbit/s.

2. Device and Circuit Configuration

We used InP/InGaAs DHBTs with a collector thickness of 200 nm [7]. The emitter size was 0.8 x 3 μm^2. The DHBTs had a base-pad isolation structure to reduce the extrinsic collector-base capacitance. The current gain (β) was 19. Figure 1 shows the typical dependence of f_T, f_{max} and total collector capacitance C_{bc} on J_c at a collector-emitter voltage of 1.2 V. The maximum f_T and f_{max} values were 271 and 343 GHz at a J_c of 3.5 and 2.8 mA/μm^2, respectively. A low C_{bc} of 8 fF was maintained until it gradually increased at a J_c of over 4 mA/μm^2.

We designed two types of selector IC with different J_c values; a J25 selector and a J50 selector. The former has a J_c of 2.5 mA/μm^2, at which f_T and f_{max} are almost maximum. The latter has a J_c of 5.0 mA/μm^2. The J_c of the J50-selector is double that of the J25-selector while the f_T and f_{max} of the J50-selector are decreased by 15 % and 35 %, respectively. The circuit configurations of the J25-selector and the J50-selector are identical. Figure 2 shows the circuit diagram of the selector IC. It consists of three input buffers and a selector core, which are configured with an emitter-coupled logic (ECL). The input buffers are DC-coupled and include a cascode-type differential amplifier with a logic swing of 400 mV. In the amplifier, we obtain the same logic swings for both the J25- and J50-selectors by adjusting the load resistor values. The selector core is a conventional series-gated type and drives external 50-Ω loads directly. For both the ICs, the logic swing of the selector core is 300 mV and the internal load resistors are 50 Ω. Here, in order to obtain the same logic swing with the same internal load resistors, the J25-selector uses two parallel transistors while the J50-selector uses only one because of its high J_c. This is a merit of the J50-selector in terms of reducing the occupied area and relaxing the fan-out driven by the input buffers. The supply voltage (V_{EE}) is designed to be -5.0V. Both ICs are 1.5 x 1.5 mm^2 in size.

3. Experiment

The selector ICs were evaluated on a wafer by using a 100-Gbit/s multiplexing operation. The inputs were a 50-GHz sinusoidal clock and two sets of 50-Gbit/s pseudorandom bit sequence (PRBS) data generated by an in-house pulse-pattern generator (PPG) [8]. In order to obtain a true 100-Gbit/s PRBS at the selector outputs, the phase difference between the two PRBS was set at half-PRBS periods. All the inputs were single-ended, and their amplitudes were 1 V_{pp}. Selector outputs were observed using a 70-GHz bandwidth sampling oscilloscope. Figures 3 and 4 show the 100-Gbit/s output waveforms of the J25- and J50-selectors, respectively, at the designed V_{EE} of -5.0 V. Although both the ICs output a 2^7-1 PRBS pattern, which features seven consecutive identical digits (CIDs) followed by six CIDs such as "0000000111111" (Figs. 3 and 4(b)), clear eye openings were obtained only for the J-50 selector. This means that the J50-selector operates faster than the J25-selector and that increasing J_c at the expense of f_T/f_{max} is an effective way to increase the operating speed of the InP DHBT IC.

To examine the speed limit of the J50-selector, we conducted measurements at over -100 Gbit/s using our PPG [8] while adjusting V_{EE}. Figure 5 shows 100- and 145-Gbit/s operating waveforms at a V_{EE} of -4.5V, at which the J_c and the logic swing of the selector core decreased to 4.4 mA/μm^2 and 260 mV, respectively. Fine 100-Gbit/s eye openings with an RMS jitter of 400 fs and 145-Gbit/s eye openings were confirmed. The operating speed of 145-Gbit/s is comparable to the fastest speed reported for an InP HEMT selector IC [5]. The power consumption was 1.5 W at a V_{EE} of -4.5V.

4. Conclusion

We confirmed experimentally that increasing J_c at the expense of f_T/f_{max} is an effective way of enhancing the speed of an InP DHBT IC in the 100-Gbit/s region. As a result, fine 100- and 145-Gbit/s eye openings were obtained for an InP

DHBT selector IC designed with a high J_c.

Acknowledgments
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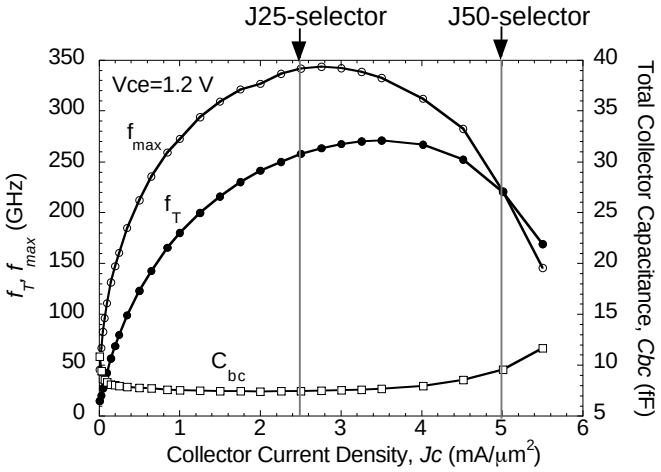

Figure 1. Typical dependence of f_T, f_{max}, and total collector capacitance on collector-current density at V_{CE} of 1.2V.

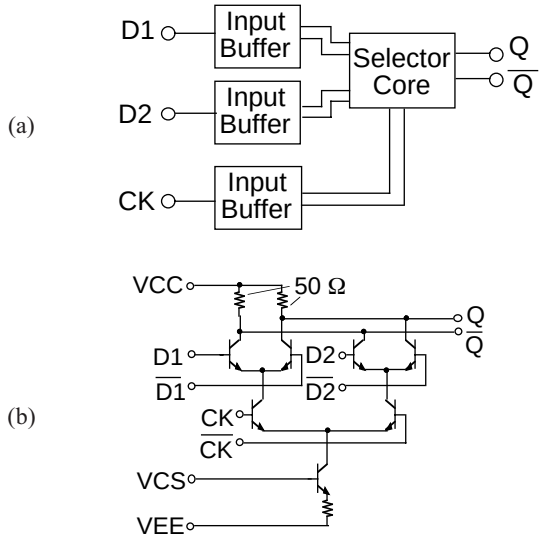

Figure 2. Circuit diagram of selector ICs.
(a) Block diagram, (b) Circuit diagram of selector core.

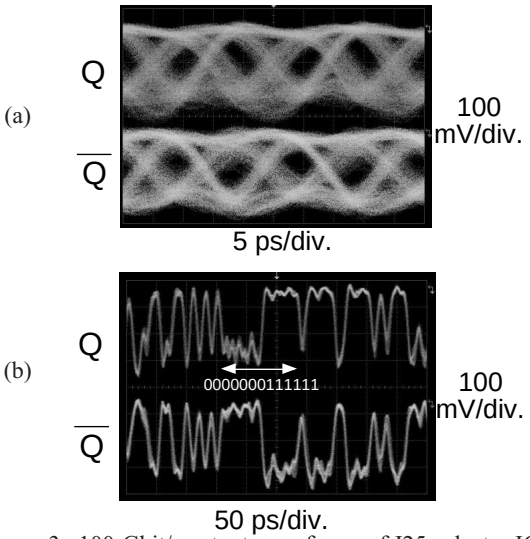

Figure 3. 100-Gbit/s output waveforms of J25-selector IC. (V_{EE}=-5.0V) (a) Eye pattern, (b) 2^7-1 PRBS pulse pattern

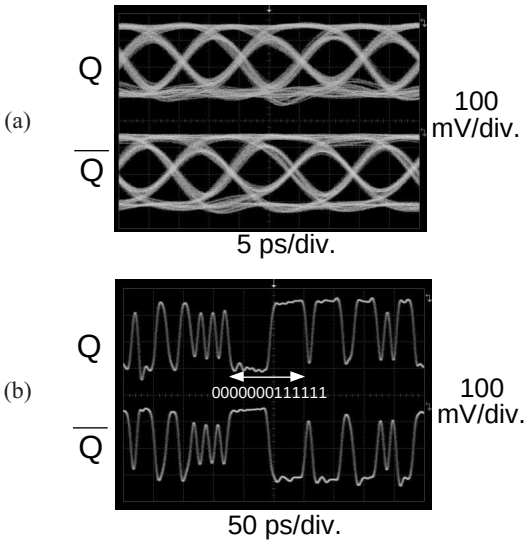

Figure 4. 100-Gbit/s output waveforms of J50-selector IC. (V_{EE}=-5.0V) (a) Eye pattern, (b) 2^7-1 PRBS pulse pattern

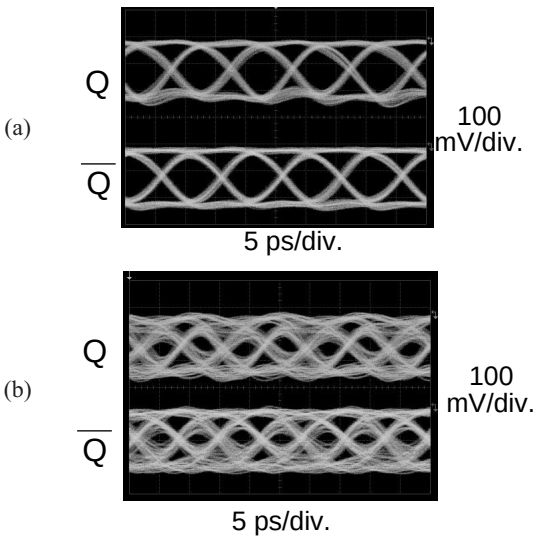

Figure 5. Output waveforms of a J50-selector IC with a reduced V_{EE} of -4.5 V. (a) 100 Gbit/s, (b) 145 Gbit/s