

**G-8-1 (Invited)****Rapid Prototyping of Quantum Circuits Using Erasable Electrostatic Lithography**

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**1. Introductions**

Over the last decade there has been extensive research on quantum transport in devices that are small in comparison to some important physical length scale. This research has led to studies of ballistic one dimensional transport and single electron effects in quantum dots. More recently these devices have been proposed as building blocks for solid state implementation of quantum computing architectures.

One of the key problems associated with quantum computing research is that the quantum devices are very sensitive to disorder. Charges of impurities can cause quantum states to shift in energy, or fluctuations in charge can lead to loss of quantum coherence and therefore information.

In this paper we will demonstrate a new technique for creating sub-micron quantum transport devices, using a low temperature atomic force microscope (AFM) tip to deposit charged lines on a GaAs GaAlAs heterostructure device containing an high mobility two dimensional electron gas (2DEG) 100nm below the surface. The charge is deposited in a dilution refrigerator at 25 mK. The charge is localized and remains immobile for months. The density of trapped electrons can be made large enough to deplete out the electrons in the underlying 2DEG.

Using this technique lines of negative charge drawn on the surface are used to create sub-micron conducting paths in the underlying 2DEG. IN this manner quantum dots, 1-D ballistic channels and large quantum dots can be fabricated and measured in the dilution refrigerator at 25 mK. We also show that using

a light emitting diode (LED) we can erase the localized charge pattern on the surface of the heterostructure. The 2DEG then returns with no defined conducting pathways remaining. Thus we have a technique for erasing the quantum structures so that a different quantum device can be fabricated. We call this type of lithography electrostatic erasable lithography (EEL) [1].

**2. Fabrication of quantum devices**

The starting devices to be investigated consisted of a GaAs GaAlAs heterostructure which is patterned using optical lithography to define a hall bar mesa structure with source and drain contacts. Optical lithography is also used to define gate structures on top of the MESA. In this example we then defined a 1 micron long by 0.7 micron wide split gate using electron beam lithography techniques. We finally spin on a layer of PMMA electron-beam resist which is then patterned using electron beam lithography to provide alignment marks. The alignment marks allow the AFM to find the sub-micron split gate at 25 mK. Once this is located we use a negative voltage on the tip to deposit charge on the surface. We need the tip to make contact with the surface and a voltage of -6V on the tip is required to leave the 2DEG completely depleted when the tip is withdrawn.

In figure 1 (b) we show how a dot of charge deposited in between the split gate alters the conductance of the channel both as a function of tip position above the sample and as a function of voltage on the tip. Figure 1 (c) and (d) show that deposited negative charge remains months after an initial limited decay,

but charge from a positive tip leaks away in a few minutes.

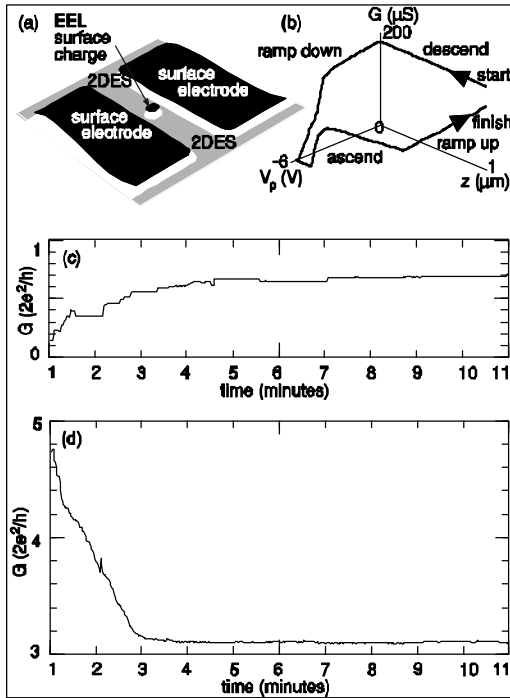


Figure 1. (a) Schematic of the split gate with region of charge defined in the middle. (b) 3D plot of conductance through the channel as a function of tip height and voltage. (c) and (d) show the conductance variation with time after charge deposition.

### Quantum devices studied

In order to demonstrate this technology we defined two 1-D channels parallel to each other in the middle of the large e-beam defined split gate. We then erased this and defined one narrow 1-D constriction within the larger 1-D channel showing well defined 1-D quantized plateaus to be observed. When this was erased we defined a quantum dot within the 1-D channel. All these devices were defined measured and then erased at 25 mK. We use a negative voltage on the conducting tip of the AFM when not in contact to modify the conductance of the device. The variation in the conductance as a function of tip position is used to image the conducting pathways defined by the EEL.

### 3. Imaging quantum chaotic orbits in a large quantum dot

We go on to show how we can use the EEL technique to define a large quantum dot which is open to the source and drain reservoirs. The dot is 2 microns long by 1 micron wide. We use scan gate imaging to map out the fractal nature of the transport property in the large quantum dot. We see that the scan gate images are extremely sensitive to magnetic field so that the addition of a fraction one magnetic flux quanta into the dot makes the images change substantially. The correlation between images oscillates with a period of one flux quanta being added into the dot area [2].

With some imaging processing of these scan gate images we are able to create images which are strongly reminiscent of computer models predicting the charge density expected in such dots including scarred wavefunctions..

### Conclusion

We demonstrate that a low temperature conducting tip AFM can be used to rapidly prototype sub-micron quantum devices, allowing the variation of quantum transport phenomena to be studied as a function of sample geometry. This technique is ideally suited to correcting for disorder effects when trying to construct quantum computing devices and for rapid prototyping of quantum architectures.

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### References

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