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Room Temperature Operation of an Exclusive-OR Circuit Using a Highly-Doped Si Single-Electron Transistor

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1. Introduction

Single-electron devices utilizing the Coulomb blockade effect are promising for use as the basic elements of future low-power and high-density integrated circuits.[1-4] To develop these devices into commercial products, a room temperature operation capability and a Si construct are necessary.

Single-electron transistor (SET) applications to logic circuits need to have more advanced functional features than the features which conventional metal–oxide–semiconductor (MOS) circuits have. Takahashi *et al*.[5] reported an exclusive-OR (XOR) circuit operation using a Si SET fabricated by a pattern-dependent oxidation at 40 K. They utilized the Coulomb oscillation and the ability of a SET to contain several gate electrodes. Saitoh *et al*.[6] reported an XOR circuit operation using a point-contact channel single-hole transistor with a single dot at room temperature. Recently we have fabricated highly-doped Si SET with a series of geometrically defined multiple islands and multiple side gates.[7] Highly-doped SETs have the advantage of being easy to fabricate because it requires only one electron beam (EB) mask to form Coulomb islands and the double side gates. Moreover, SETs with serially connected multiple Coulomb islands have the advantage both for high temperature operation[8] and the suppression of cotunneling. Using the SET, we have also reported an exclusive-Not-OR (EXNOR) circuit operation at 77 K using this SET.[9]

This time, a large peak-to-valley current ratio (PVCR) of Coulomb oscillation was observed even at room temperature in the SET with the multiple Coulomb islands. Therefore, in this study, using the room temperature characteristics, we report an XOR operation at room temperature. Since the SET with multiple gates reduces the number of required transistors for the logic circuit compared with using conventional complementary MOS transistors, the room temperature operation and easy fabrication of the circuit should open up the development of SET logic circuits.

2. Device Fabrication

We fabricated a one-dimensional regular array of 22 nanoscale islands in an SOI layer using EB lithography. Figure 1(a) shows the schematic of the SET. Multiple gates (indicated as Gate1 and Gate2) were formed at both sides of the channel wire. Doping of the top Si layer was carried out by $POCl_3$ diffusion at 800 °C. The doping level was about 2 x 10^{19} cm^{-3}. After dry etching by using an electron cyclotron resonance etcher with the resist pattern as a mask, subsequent isotropic wet etching in a $NH_4OH/H_2O_2/H_2O$ solution was conducted to reduce the dimensions of the device.[10] The final thickness of the top Si layer was about 20 nm. After the wet etching [Fig.1(b)], the width of the island and that of the region between adjacent islands were about 20 and 10 nm, respectively. The distance between the centers of adjacent islands was 250 nm and the length of the narrow channel wire region (~10 nm) between adjacent islands was about 50-100 nm. The separation between the channel wire and the side gates was 240 nm.

3. Coulomb oscillation of SET with multiple islands

Figure 2 shows Coulomb oscillations of SET with a single island (a) and with 22 islands (b) at room temperature. The maximum PVCR observed is 3.5 in SET with a single island (a) and 77 with 22islands. We found a tendency that SETs with multiple islands have larger PVCR than SETs with a single island. Large PVCR is advantageous to circuit operations.

4. Application to XOR operation at room temperature

The SET with multiple gates can operate as an XOR by utilizing the oscillatory drain current (I_d) characteristics (Coulomb oscillation). Figure 3(a) shows an equivalent circuit of our SET with multiple (double) gates. Figure 3(b) shows operation principle of the SET with multiple gates. The I_d oscillation is determined by the sum of the products of each gate capacitance (C_{gi}) and gate voltage (V_{gi}). When C_{g1} is equal to C_{g2}, I_d is simply a function of the sum of V_{gi}.

Figure 4(a) shows the I_d characteristics of our SET with 22 islands at room temperature as a function of V_{g1} or V_{g2}. Here, the voltage of only one of the side gates was swept with the other side gate voltage kept 0 V. As seen in the figure, the characteristics with V_{g1} are nearly equal to those with V_{g2}. This indicates that C_{g1} almost equals C_{g2}, which enables an easy application of our SET to the XOR logic circuit. The I_d peak appears when the gate voltage is about 34.3 V, and the I_d valley appears when the gate voltage is about 38.6 V. We chose the low (L) and high (H) input voltages for one side gate to be 15 and 19.3 V, respectively, for the XOR operation. Then, the sum of the voltages of the two side gates becomes 30 and 38.6 V for the LL and HH input gate voltage states, respectively. For the LH and HL input states, the sum becomes 34.3 V.

Figure 4(b) shows the I_d switching in response to the

switching of the two input gate voltages between 15 V (L) and 19.3 V (H) at room temperature. When the input voltages are the LL and HH states, the output I_d is L (smaller than 0.3 pA). When the input voltages are the LH and HL states, the output I_d is H (higher than 0.6 pA). These results demonstrate a successful XOR operation in our SET circuit.

5. Summary

We fabricated a highly-doped Si SET with multiple islands and multiple side gates. The SET exhibited Coulomb oscillation with large PVCR at room temperature. We applied the Coulomb oscillation and the multiple gate input characteristics to an XOR operation and achieved a successful I_d switching at room temperature. Using an SET with multiple gates requires having fewer transistors in a logic circuit compared with a circuit composed of conventional CMOS transistors. Besides that advanced functional feature, easy fabrication and room temperature operation of our proposed circuit prove the feasibility of practical SET logic circuits.

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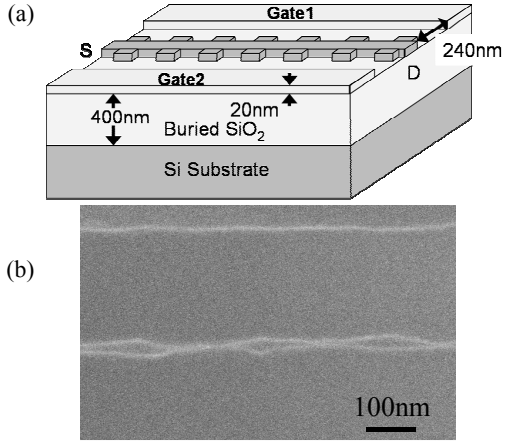

Fig.1 (a) Schematic diagram and (b) SEM image of the SET having double side gates and a highly doped narrow channel with an array of nanoscale islands.

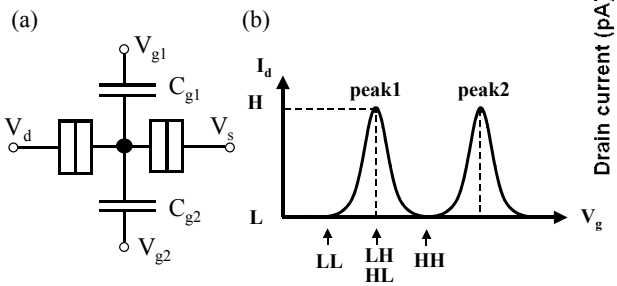

Fig.3 (a) Equivalent circuit of our SET with double gates. C_{gi} and V_{gi} stand for gate capacitance and voltage, respectively. V_d and V_s are drain and source voltages. V_s is grounded. (b) Operation principle of the SET with multiple gates. When the sum of the two input voltages becomes a voltage where peak appears, the drain current (I_d) increases (high (H) output state). On the other hand, when the sum becomes a voltage where a valley appears, I_d decreases (low (L) output state).

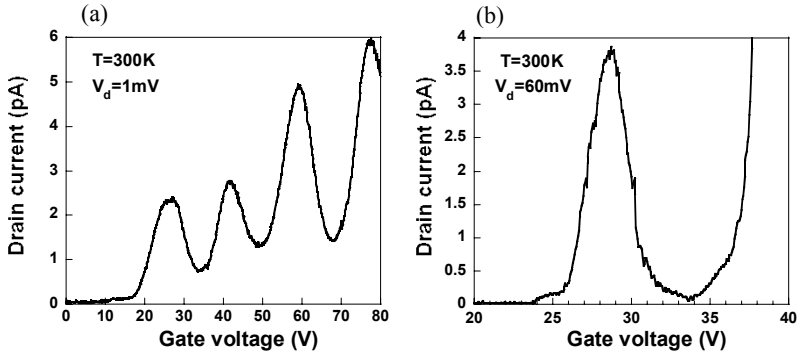

Fig.2 Drain current *vs* gate voltage characteristics of SET with (a) a single island and (b) 22 islands at room temperature. The observed maximum PVCR is (a) 3.5 and (b) 77.

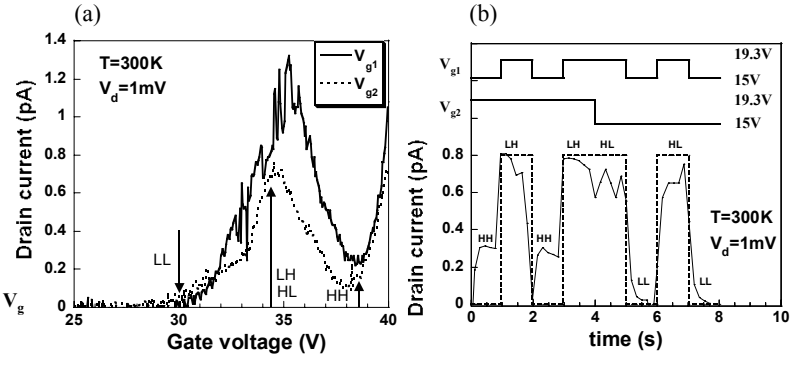

Fig.4 (a) Drain current (I_d) *vs* gate voltage characteristics of SET with 22 islands at room temperature. The solid and the broken lines are characteristics shown as a function of V_{g1} and V_{g2}, respectively. (b) Measured I_d switching characteristics when the input gate voltages (V_{g1} and V_{g2}) are switched between 15 and 19.3 V at room temperature. Dotted line shows the ideal output current of XOR circuit.