

H-2-1 (Invited)**Silicon Quantum Tunneling Devices – FIBTET and MOSET**

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1. Introduction

As CMOS dimensions are aggressively scaled down to nanoscale regime, many device parameters such as gate oxide thickness and junction depletion width are approaching physical limits, which results in the degradation of device performance and the increase of system power density. The physical origins of these CMOS limits are primarily in the quantum effects such as tunneling currents, which leak through the ultra-thin gate insulator or the heavily doped body-to-drain junction. Therefore, for the design of the nanoscale electron devices, a novel methodology to actively exploit these inevitable tunneling currents as the operation principle of the device is strongly required. This paper describes SOI CMOS-based quantum-tunneling devices exploiting band-to-band tunneling between channel and source/drain region.

2. FIBTET

The fabricated quantum-tunneling devices have a structure totally compatible with SOI CMOS device except for degenerate channel doping and the intentional omission of lightly doped drain (LDD) region (Fig. 1(a)). Heavy channel doping concentration creates the degenerate Fermi level in the channel region of the self-aligned SOI MOSFET and consequently enables inter-band tunneling between degenerate channel and source/drain (Fig. 1(b)). The key principle of the device operation is the field-induced band-to-band tunneling effect and thus, the name of this quantum-tunneling device is “FIBTET” – field induced band-to-band tunneling effect transistor. In the transfer I - V characteristics of FIBTET (Fig. 2(a)), negative-differential transconductance (NDT) characteristics have been observed at room temperature. By controlling the critical device parameters such as gate oxide thickness to enhance the field effect, the peak-to-valley current ratio over 5 has been obtained at room temperature and the negative-differential conductance (NDC) characteristics as well as NDT have been observed in the output I - V curves of the same FIBTET (Fig. 2(b)). In addition, FIBTETs demonstrate the complementary NDT and NDC characteristics at room temperature both for n -FIBTETs with p^+ -channel and n^+ -source/drain and p -FIBTETs with n^+ -channel and p^+ -source/drain [1,2]. The size dependence of the device characteristics shows that the peak tunneling current increases according to the increase of the channel width (the increase of tunneling area), and to the decrease of the channel length due to the reduced transit time in channel region [2]. These channel size dependencies indicate that the electrical parameters of FIBTET such as the peak tunneling current can be controlled by the 2-dimensional layout design of channel dimensions.

In terms of the application to ultra-low power, ultra-high density nanoelectronic circuits, an XOR logic circuit using one transistor (1T) has been demonstrated as a novel circuit scheme utilizing tunneling currents in nanoscale electronic devices. Based on NDC characteristics controlled by NDT peak and valley

voltage in one transistor (Fig. 3(a)), the basic operation of 1T XOR logic function is demonstrated at room temperature for digital logic application (Fig. 3(b))

3. MOSET

In principle, FIBTETs can exhibit Coulomb blockade effect based on single-electron tunneling mechanism in their structure, since channel region can act as a quantum-dot connected to the source and drain via p^+ - n^+ tunnel junctions. If we shrink the size of the FIBTET channel region to the quantum dot level and the environmental temperature decreases, Coulomb blockade oscillations can be observed in FIBTET structure. Thus, this device becomes MOS-based single-electron transistor (SET) – “MOSET”. The clear rhombus-shaped valleys caused by the Coulomb blockade are observed in FIBTETs at $T = 77$ K (Fig. 4(a)), while normally doped sample shows typical SOI MOSFET characteristics (Fig. 4(b)). These suggest that the observed single-electron phenomena can be attributed to the degenerately doped island with the Fermi level in the valence band between the two p^+ - n^+ tunnel junctions. From Fig. 4(a), the single-electron addition energy, E_a , and total capacitance, C_Σ , are estimated to be 79.2 meV ($\sim 10k_B T$) and 2.02 aF, respectively.

Three primary peaks and valleys, which maintain their number even at high V_{ds} , imply that the degenerate Si QD has three available energy states in the range of energy band overlap (Fig. 5). Coulomb oscillations were observed even at 220 K by a geometrically well-defined island and two p^+ - n^+ tunnel junctions in the self-aligned structure by the conventional CMOS technology (Fig. 6) [3]. Considering the value of charging energy and channel (dot) size, it can be concluded that the channel length, width, and SOI thickness should be scaled down to 10 nm for the achievement of the room temperature operation with the single-electron addition energy $E_a \sim 1$ V, which is sufficient for practical applications.

4. Conclusions

We have implemented silicon quantum-tunneling devices – FIBTET and MOSET exploiting junction band-to-band tunneling in SOI CMOS devices with a degenerately doped channel region. FIBTET shows room temperature NDT and NDC characteristics regardless of channel dimension. Using these characteristics of FIBTET, 1T XOR logic has been demonstrated at room temperature. Furthermore, FIBTETs with mesoscopic channel dimensions can provide Coulomb blockade effect as an SET (MOSET) at low temperature.

Acknowledgements

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References

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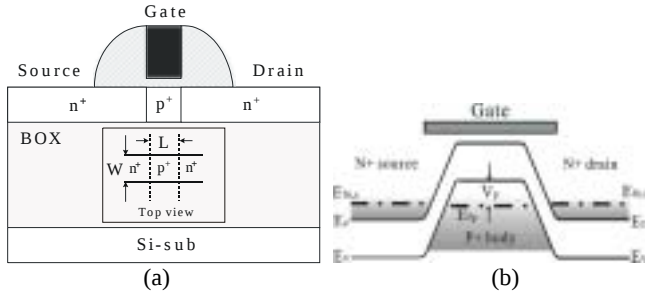


Fig. 1. (a) Cross-sectional schematic of the fabricated n-FIBTET. (b) Schematic energy band diagram of n-FIBTET under the gate along the channel at thermal equilibrium state.

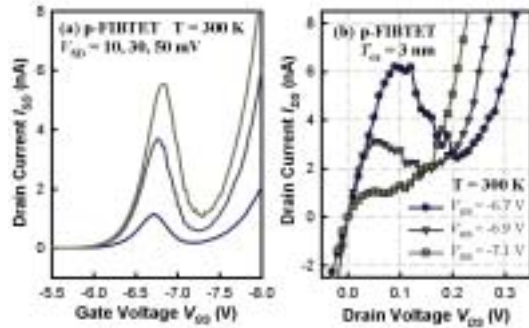


Fig. 2. Electrical characteristics of the fabricated p-FIBTET at 300 K: (a) Transfer and (b) output I-V characteristics.

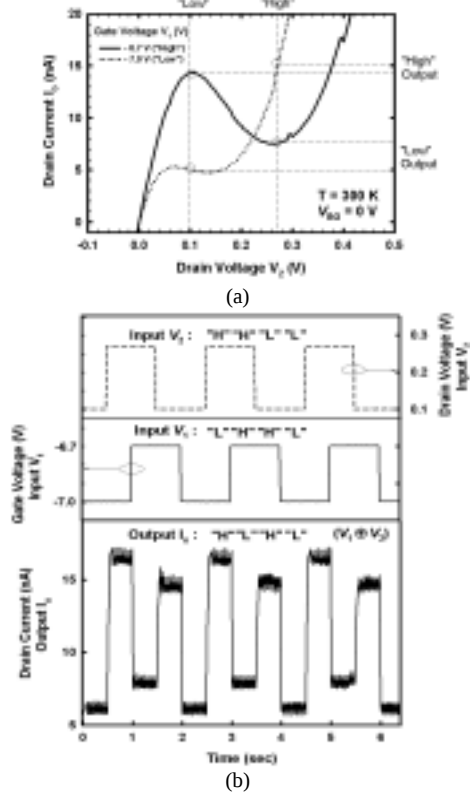


Fig. 3. (a) Measured output I_D - V_D characteristics at different V_G of p-FIBTET with $L = 50$ nm and $W = 200$ nm at room temperature. (b) Measured transient waveforms of V_G (V_1), V_D (V_2), and I_D (I_0) at room temperature.

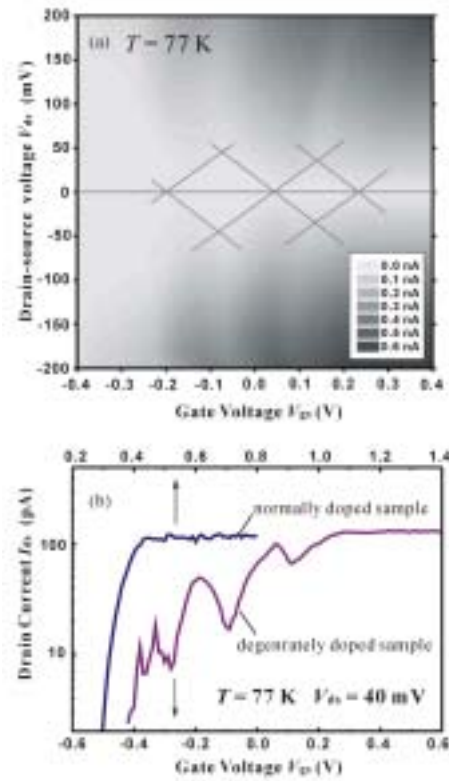


Fig. 4. (a) Contour plot of the drain current as a function of drain and gate bias and (b) I_{ds} - V_{gs} characteristics at 77 K for normally doped ($\sim 10^{18} \text{ cm}^{-3}$) and degenerately doped ($\sim 10^{20} \text{ cm}^{-3}$) samples. $V_{ds} = 40$ mV. ($L=W=30$ nm)

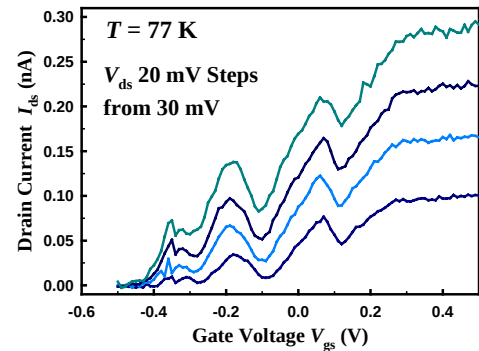


Fig. 5 I_{ds} - V_{gs} characteristics as a function of V_{ds} for a degenerately doped sample at 77 K. V_{ds} is varied from 30 to 90 mV with 20 mV steps.

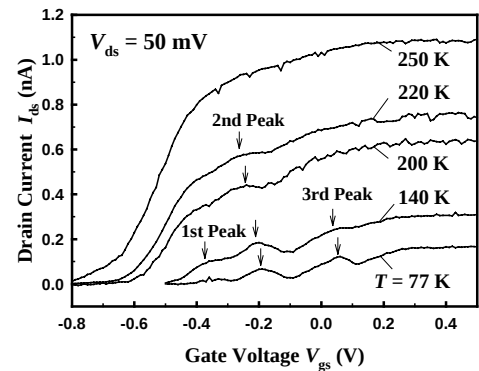


Fig. 6 I_{ds} - V_{gs} characteristics as a function of the temperature at $V_{ds} = 50$ mV. The second peak with the highest band-to-band tunneling probability was observed, even at 220 K.