SET/CMOS Hybrid Integration Process for Multiple-Valued Logics

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1. Introduction

Single-electron transistor (SET) is a promising device for future applications to low-power multiple-valued logics (MVL) and memory [1,2]. However, it has not yet been clear how to overcome the effect of the inherent drawback of SETs (temperature dependent PVCR degradation) on the system stability. Previously, we have shown by simulation that the SET/CMOS complementary-biased scheme could enhance the stability of MVL systems [3]. Therefore, it is very important to develop an integration process suitable for the SET/CMOS complementary-biased scheme which is composed of multiphase-control SET and CMOS FET. In this work, we developed an integration process for multi-phase-control SET and CMOS FET on a wafer.

2. Device Fabrication

Fig. 1(a) shows a layouts of SET, nMOSFET, and pMOSFET with bias electrodes in which V_{cg} and V_{sg} represent the control gate and sidewall gate bias of depletion gate type SET [4]. Sidewall depletion gate SET is reported to be adequate for SET/CMOS hybrid logic due to its logical versatility originated from multiphase-control nodes, V_{cg} and V_{sg} [4].

The devices are fabricated on lightly doped p-type (100) SOI wafers. For the formation of active regions of CMOS and SET, conventional photolithography with ArF light source is employed. The Si wire is shrunk through the following processes: photoresist (PR) trimming by O_2 plasma, reactive ion etching (RIE), and isotropic chemical etching. After Si nanowire formation, 15-nm-thick SiO₂, 70-nm-thick Si₃N₄, and 50-nm-thick SiO₂ layers are deposited. Following the anisotropic 2-step RIE and oxide stripping, nitride groove is made as shown in Fig. 1(b). After the formation of nitride groove, CVD oxide is deposited. Then, sidewall depletion gates are formed along the nitride groove, through the n+ poly-Si deposition, lithography, and anisotropic RIE.

For the electrical isolation between side gates and the control gate, 10-nm-thick oxide is deposited. On the other hand, the deposited oxide in CMOS region which is outside of dual-gate-oxide (DGOX) mask shown in Fig. 1(b) is eliminated by HF solution, then thin gate oxide with 3.7 nm thickness is thermally grown. Thin oxide formation for CMOS transistors is necessary for achieving the high output resistance.

Poly-Si gates for both SETs and CMOS transistors are formed simultaneously. Then, oxide and nitride under the extension of poly-Si control gates of SETs are stripped for the following source/drain implantation. After RTA, back-end processes including contact hole formation and metallization are performed.

Fig. 1(c) and (d) shows SEM images of cross section along the channel length and width direction of fabricated SET,

respectively. Major geometric parameters are represented in the figure; Width, length, and height of quantum island is 20 nm, 40 nm, and 10 nm respectively.

3. Results and Discussion

Fig. 3 shows the drain current of SET as a function of control gate voltage V_{cg} . Coulomb oscillation peaks are clearly observed at 4.2K with a period ΔV_{cg} of 100 mV. The Coulomb oscillation is originated from the two electrically induced tunnel junction and Si quantum-island. C_{cg} (capacitance between control gate and quantum-island) is extracted to be 1.6 aF from the calculation of $e/\Delta V_{cg}$. As shown in Fig. 4, the position of oscillation peak is shifted to the left as V_{sg} increases, which is the typical characteristic of depletion gate type SETs [4].

Fig 5. shows the transfer characteristics of CMOS transistors of which width and length are 1 μ m. The threshold voltages are 0.3 V and -0.65 V for nMOS and pMOS transistor, respectively. Also, it is noticed that output resistances from drain nodes of CMOS transistors are very high, which is prerequisite in SET/CMOS hybrid logic to guarantee the sufficient voltage gain [3]. By simple extraction from the transfer curve, we can estimate that output resistances are over 1 G Ω for both MOSFETs at typical current level of SET/CMOS hybrid logic, $I_D <1$ nA. Such a high output resistance is attributed to the thin gate oxide formation for the CMOS region defined by DGOX mask.

Through the SPICE simulation based on the model parameter extracted from the measured data, we confirmed that SET/CMOS hybrid logic implemented by the fabricated devices accomplish a correct function [4,5]. Fig. 6 show a schematic diagram of complementary-biased universal literal gate and its transfer characteristic. The side gate voltages of SETs, V_{sgo} and V_{sge} , are biased so that the SET in biasing stage generates an odd mode current (I_{odd}) and the SET in gain stage drives an even mode current (I_{even}). The pMOSFET current mirror duplicates the complementary current, I_{odd} , to the driving stage as a current load. As V_{in} increases, Coulomb oscillation of SET produces output voltage transitions at each cross point of I_{even} and I_{odd} .

3. Conclusions

Both SET and CMOSFET were fabricated successfully on a wafer. The SET shows multi-phase-controlled Coulomb oscillations and the CMOS transistors show very high output resistance, which are essential requirements for the SET/CMOS complementary-biased logic. Consequently, it is demonstrated by simulation that the stability-enhanced SET/CMOS hybrid circuits can be implemented by the fabricated devices.

References

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Fig. 1 (a) Layout of SET/CMOS hybrid devices and (b) key process steps.



Fig. 2 SEM images of cross-section of SET along the (a) channel length and (b) width direction.



Fig. 3. Coulomb oscillation at at $V_d = 5$ mV.



Fig. 4. Oscillation shift by depletion gate bias, V_{sg} , at $V_d = 1$ mV.



Fig. 5. Transfer characteristics of CMOSFETs.



Fig. 6 (a) Universal literal gate implemented by complementary -biased scheme and (b) its transfer characteristic at 27K