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Room-Temperature Demonstration of Low-Voltage Static Memory Based on Negative Differential Conductance in Silicon Single-Hole Transistors

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1. Introduction

Rapid progress in the fabrication techniques of silicon single-electron transistors (SETs) and single-hole transistors (SHTs) has made it possible to observe large Coulomb blockade (CB) oscillations even at room temperature (RT) [1,2]. In RT-operating SETs or SHTs with an ultra-small dot, quantum mechanical effects such as negative differential conductance (NDC) appear. Very recently, we have succeeded in the first RT observation of NDC in a multiple-dot SET [3] and a single-dot SHT [2]. Although most of the conventional SET/SHT circuit design had not considered the quantum effects, we proposed and demonstrated highly-functional logic operation using NDC observed in RT-operating SHTs for the first time [2]. On the other hand, NDC characteristics in resonant tunneling diodes (RTDs) or Esaki diodes have been extensively studied for static memory applications [4-7]. Although the number of devices constructing one memory cell can be significantly reduced in the proposed NDC-based static memories, it is very difficult to integrate them into the existing CMOS VLSI due to their vertical structures.

In this paper, we propose a new static memory based on NDC in RT-operating SHTs. We fabricate an SHT showing NDC and a load pMOSFET on one chip. Gate-controllable latch operation at low supply voltage is demonstrated at RT.

2. Fabrication and Device Characteristics

An SHT is fabricated in the form of a p-type ultra-narrow wire channel MOSFET [2]. The extremely narrow channel is formed on a 20-nm-thick SOI by EB lithography, anisotropic etching using TMAH and isotropic etching using SC1 ($NH_4OH/H_2O_2/H_2O$). After wet etching, the wire channel is slightly oxidized. The thickness of the thermal gate oxide is 10 nm. Additional 35-nm-thick gate oxide is deposited by LP-CVD. The channel length is 90 nm, and the final channel width and height are estimated to be less than 5 nm. A dot and tunneling barriers are self-formed in the constricted channel, and the device acts as an SHT [2].

Fig. 1 shows the RT I_d-V_g characteristics of the fabricated SHT. All the measurements in this paper were performed at RT. Large CB oscillation with the peak-to-valley current ratio (PVCR) of 10.5 is observed. Fig. 2 shows the RT I_d-V_{ds} characteristics of the same device at various V_g. At V_g of -0.3 V, clear NDC with the PVCR of 6.5 is observed. As V_g is decreased, the NDC peak shifts to lower V_{ds}. This controllability of NDC curves by V_g is the prominent feature of NDC in SHTs [2].

3. Room-Temperature Latch Operation

We propose a new type of static memory using NDC observed in RT-operating SHTs. For demonstration of basic latch operation, we construct the circuit illustrated in Fig. 3. The SHT showing NDC (Fig. 2) is serially connected to a load pMOSFET which was fabricated on the same chip. Fig. 4 shows the load curve diagram of this circuit when $V_{g\text{-SHT}}$ is -0.4 V and V_{dd} is increased. The gate bias of the load pMOSFET ($V_{g\text{-MOS}}$ - V_{dd}) is fixed at -5 mV. For load curves A and C, there is only one stable operation point. But, there are two stable points for the curve B.

Figs. 5 and 6 show the measured I-V_{dd} and V_{out}-V_{dd} characteristics where V_{dd} is scanned from 0 V to 0.5 V and back to 0 V. Hysteresis appears in the range where two stable points exist in the load curve diagram. When $V_{g\text{-SHT}}$ is -0.4 V, two stable V_{out} (0.07 V and 0.17 V) exist (that is, 1 bit can be stored) for V_{dd} of as low as 0.2 V. Moreover, V_{dd} range where hysteresis appears can be controlled by $V_{g\text{-SHT}}$ and ($V_{g\text{-MOS}}$ - V_{dd}).

4. Discussions

Since one of the stable points for the curve B is inevitably located near the NDC peak in Fig. 4, large current flows at the standby mode in the circuit of Fig. 3. To overcome this problem, the configuration of serially-connected two SHTs (Fig. 7) can be adopted. In the load curve diagram (Fig. 8), both stable points are located near the NDC valleys, and thus standby currents are suppressed.

Here, we discuss the advantages of this SHT memory. First, this memory is highly compatible with the existing CMOS VLSI because of its silicon-based planar structure. Second, the area of the memory cell composed of two SHTs and one MOSFET (Fig. 7) is extremely small, enabling ultra-high-dense integration. Third, low-voltage operation (V_{dd} of 0.2 V) is possible. The last but the most important is the controllability of hysteresis curves by the gate, which cannot be achieved in the conventional NDC-based memory composed of two-terminal RTDs. Fig. 9 shows the measured V_{out}-$V_{g\text{-SHT}}$ characteristics for various V_{dd} in the circuit of Fig. 3. For a given V_{dd}, the noise margin can be maximized by setting $V_{g\text{-SHT}}$ in the middle of the hysteresis range. Hence, it is possible to optimize the operation point.

5. Conclusions

We have proposed a new static memory based on NDC in RT-operating SHTs, which is suitable for high-dense integration into CMOS VLSI. Gate-controllable latch operation is successfully demonstrated at the supply voltage of as low as 0.2 V at RT in the fabricated SHT-pMOSFET circuit.

References

[1] K. Uchida et al., *Tech. Dig. IEDM*, p.863, 2000. [2] M. Saitoh and T. Hiramoto, *Tech. Dig. IEDM*, p.753, 2003. [3] M. Saitoh and T. Hiramoto, *Jpn. J. Appl. Phys.* **43**, L210 (2004). [4] T. Mori et al., *Jpn. J. Appl. Phys.* **33**, 790 (1994). [5] J. P. A. van der Wagt et al., *Tech. Dig. IEDM*, p.425, 1996. [6] J. Koga and A. Toriumi, *IEEE Electron Device Lett.* **20**, 529 (1999). [7] H. Sorada et al., *Superlattices Microstruct.* **28**, 331 (2000).

Acknowledgements

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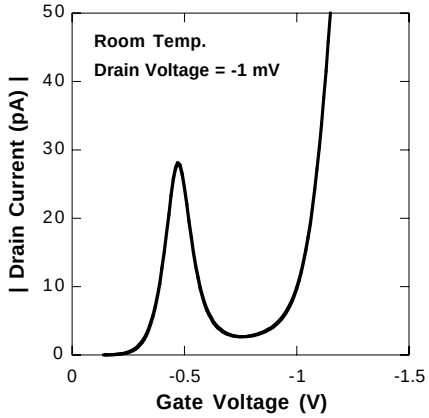

Fig. 1 : Measured RT I_d-V_g characteristics of the fabricated SHT. Large CB oscillation with PVCR of 10.5 is observed.

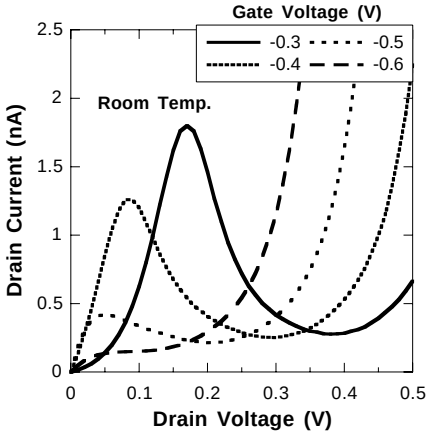

Fig. 2 : Measured RT I_d-V_{ds} characteristics at various V_g. Clear NDC with PVCR of 6.5 is observed at V_g of -0.3 V. NDC curves can be controlled by V_g.

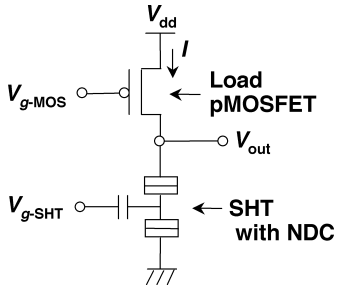

Fig. 3 : Circuit for demonstration of latch operation. The SHT and a load pMOSFET fabricated on the same chip are serially connected.

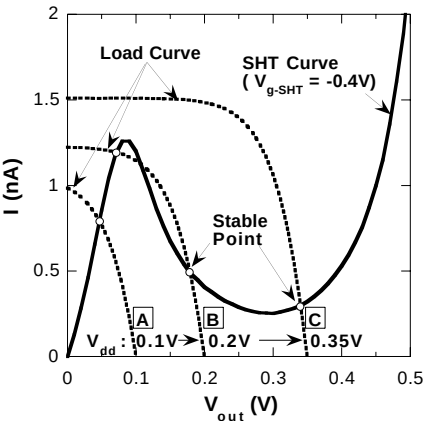

Fig. 4 : Load curve diagram of the SHT-pMOSFET latch circuit when $V_{g\text{-SHT}}$ = -0.4 V and V_{dd} = 0.1 V (curve A) / 0.2 V (B) / 0.35 V (C).

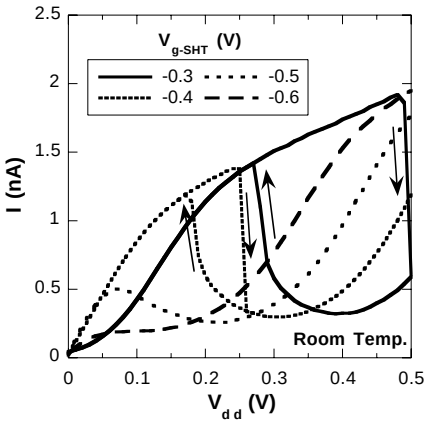

Fig. 5 : Measured RT I-V_{dd} characteristics where V_{dd} is scanned from 0 V to 0.5 V and back to 0 V. Hysteresis appears when $V_{g\text{-SHT}}$ = -0.3 V or -0.4V.

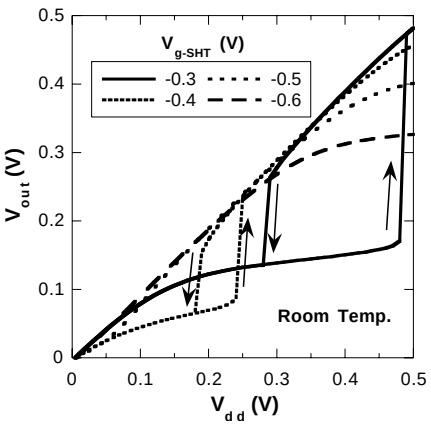

Fig. 6 : Measured V_{out}-V_{dd} characteristics at RT. Two stable V_{out} exist for V_{dd} of as low as 0.2 V when $V_{g\text{-SHT}}$ = -0.4 V. Hysteresis can be controlled by $V_{g\text{-SHT}}$.

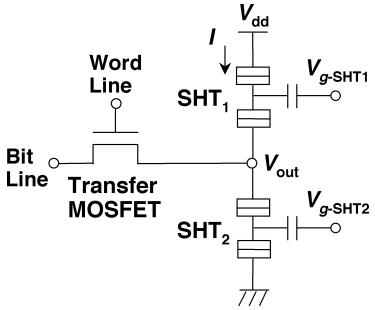

Fig. 7 : Configuration of the two-SHT NDC-based memory cell. Tranfer MOSFET for writing and reading is connected to the output node.

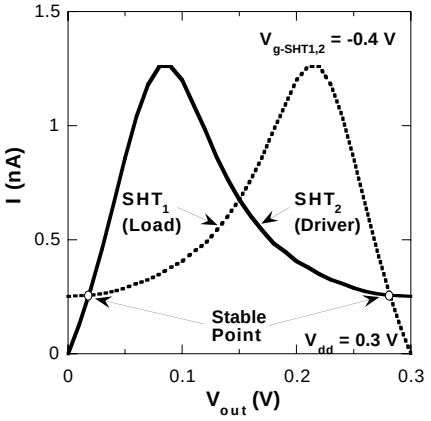

Fig. 8 : Example of load curve diagram of the two-SHT latch (Calculation). Here, it is assumed that two symmetrial SHTs whose I-V characteristics are the same as the fabricated SHT are connected.

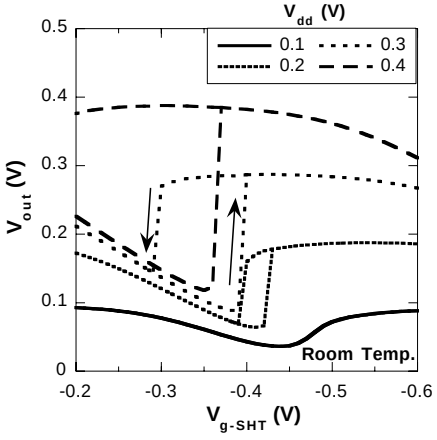

Fig. 9 : Measured RT V_{out}-$V_{g\text{-SHT}}$ characteristics in Fig. 3. $V_{g\text{-SHT}}$ in the middle of the hysteresis range maximize the noise margin for each V_{dd} (ex. $V_{g\text{-SHT}}$ of -0.35 V is optimum for V_{dd} of 0.3 V).