Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004,pp. 130-131

H-2-6

Large Threshold Voltage Shift and Narrow Threshold Voltage Distribution in Ultra Thin Body Silicon Nanocrystal Memories

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1 Introduction

Silicon nanocrystal memories [1,2] are attractive candidate for future flash memory cell structure. One of the serious problems of this memory for practical use is small threshold voltage shift(ΔV_{th}). In order to enlarge ΔV_{th}, ultra-narrow channel on an SOI substrate which causes bottleneck effect has been proposed, and it has been shown that the modification of channel structure in the channel width direction is one of the effective ways to improve memory characteristics [3]. However, it is difficult to fabricate uniform ultra-narrow channel whose width is almost the same as nanocrystal diameter by using conventional lithography. Therefore, the formation process of ultra-narrow channel can bring about the increase in fluctuations. On the other hand, the control of nanoscale SOI body thickness should be relatively easy because it is irrelevant to lithography.

In this paper, a new approach of channel structure engineering for large and uniform ΔV_{th} is experimentally demonstrated. We propose a silicon nanocrystal memory with ultra-thin and wide SOI channel. It is shown that memories with ultra-thin SOI body have larger ΔV_{th} than memories with thick body and have much smaller V_{th} fluctuations than memories with ultra-narrow channel.

2 Device Fabrication

Fig.1 shows schematics of fabricated device structures. Fig.1(a) is a silicon nanocrystal memory with ultra-thin and wide body that we propose in this paper. Fig.1(b) is a memory with ultra-narrow and thick body. The body thicknesses are 6nm and 60nm, and width is widely varied to investigate the width dependence.

The SOI thickness was adjusted by thermal oxidation and HF etching. Channel pattern was drawn by electron beam lithography. Exposed channel width of neighboring devices has 2.5nm intervals. After mesa isolation, SC1 etching (NH_4OH:H_2O_2:H_2O / 1:1:6) was performed to achieve nanoscale channel width. The channel width was estimated by the same way of Ref. [4]. Gate length is 10μm. Tunnel oxide (3nm) was formed by pyrogenic oxidation in nitrogen-diluted ambient. Oxide surface treatment was performed by HF(0.1%) dipping. Silicon nanocrystals were formed by LPCVD. Fig.2 is a SEM image of the nanocrystals. High temperature oxide (30nm) was also deposited as control oxide.

3 Basic Characteristics

Fig.3 shows the channel width dependence of initial V_{th} before writing and erasing in 60nm-thick body devices. All the measurements in this paper were performed at room temperature. Against expectation, the increase in V_{th} that is probably induced by two dimensional quantum confinement effect is observed in ultra-narrow channel devices, indicating that the SOI body thickness (height) must be far lower than the original value (60nm). This phenomenon is attributed to the problem of device isolation by reactive ion etching (RIE). Slight slope of lateral side channel caused by RIE and subsequent wet etching process may make the ultra-narrow channel a triangular structure as shown in the insets of fig.3. In ultra-narrow channel, not only the channel width but also channel height is largely fluctuated.

Fig.4 compares I_{ds}-V_{gs} characteristics after write/erase by applying $\pm$10V pulse for 500msec in two devices with body thicknesses of 6nm and 60nm. The channel width is 50nm in both devices. ΔV_{th} is apparently larger in the device with thin body (6nm).

4 ΔV_{th} Increase and Fluctuation

Fig.5 shows the channel width dependence of ΔV_{th} in memories with SOI body thickness of 6nm and 60nm. ΔV_{th} itself and its fluctuations increase as the channel width becomes narrower. This tendency is the same as the previous reports [3,5]. Moreover, the SOI body thinning along with channel width reduction can produce rapid worsening of ΔV_{th} fluctuations. However, it should be noted that thin body devices show larger ΔV_{th} than thick body devices when the channel width is the same. In thinner devices, electrons are confined in thin body and are located near silicon nanocrystals. Therefore, charges in nanocrystals can more effectively modulate the channel electron density resulting in larger ΔV_{th}. In addition, ΔV_{th} fluctuations of thin and wide channel devices are significantly suppressed compared with those of narrow channel devices, especially when the channel width is fluctuated.

Fig.6 and fig.7 show the comparison of V_{th} distribution of write/erase states between narrow channel devices (Group A in fig.5) and relatively wide and thin channel devices (Group B in fig.5). As can be seen in fig.6, the erase and write states in Group A are widely distributed and they partly overlap, making it impossible to distinguish two states. One of the reasons of such wide distributions is the two dimensional quantum confinement effect. As shown in fig.3, this effect abruptly increases initial V_{th} which is one of the criteria of write/erase V_{th}. On the contrary, devices in Group B give much narrower distribution and the two states are clearly separated, while average ΔV_{th} in Group B is as large as Group A.

5 Summary

Characteristics fluctuations in silicon nanocrystal memories induced by channel structure modification are experimentally demonstrated. Although the ultra-narrow channel enables us to obtain large ΔV_{th}, write/erase V_{th} fluctuations induced by channel width fluctuations are very difficult to control. To suppress the fluctuations, we propose a novel channel structure with ultra-thin and relatively wide channel. Memories with 6nm-thick and around 50nm-wide channel show large ΔV_{th} and uniform write/erase V_{th}. A body structure with nanometer thickness and several tens of nanometer width is one of the hopeful structures for future nanocrystal memories.

Acknowledgments

This work was partly supported by Grant-in-Aid for COE (Center of Excellence) Research (#12CE2004 "Control of Electrons by Quantum Dot Structures and Its Application to Advanced Electronics"), and Grant-in-Aid for Scientific Research, and the IT program from the Ministry of Education, Culture, Sports, Science and Technology, Japan.

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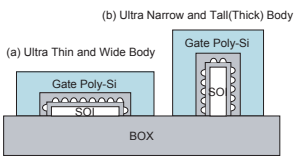

Fig. 1: Schematic cross sections of fabricated silicon nanocrystal memories.

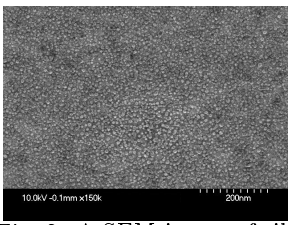

Fig. 2: A SEM image of silicon nanocrystals. The average size is about 6nm and density is 8-9×10^{11}cm^{-2}.

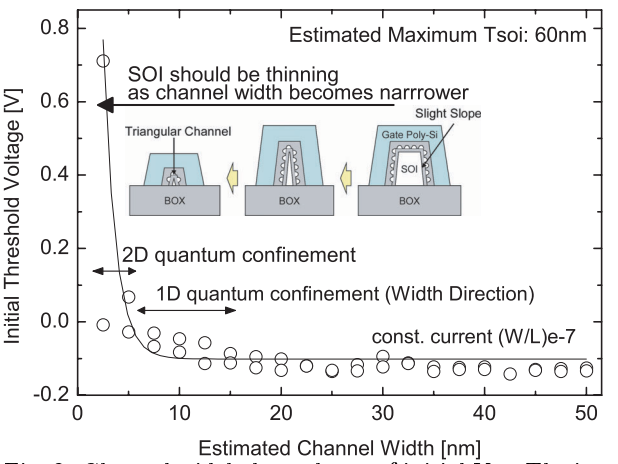

Fig. 3: Channel width dependence of initial V_{th}. The increase in V_{th} due to two-dimensional quantum confinement is observed, indicating that SOI body thickness may be unconsciously thinned when channel width is a few nanometer.

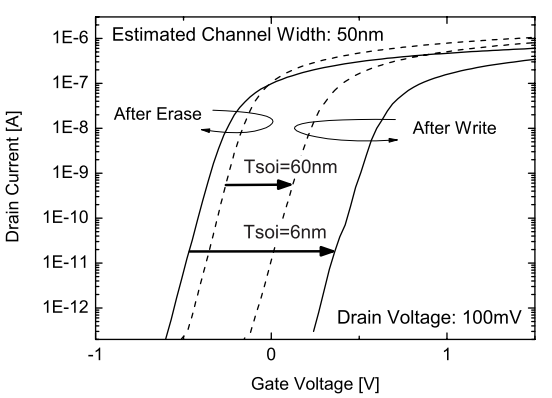

Fig. 4: I_{ds}-V_{gs} characteristics of silicon nanocrystal memories after write and erase. The increase in ΔV_{th} is observed as the body thickness becomes thinner.

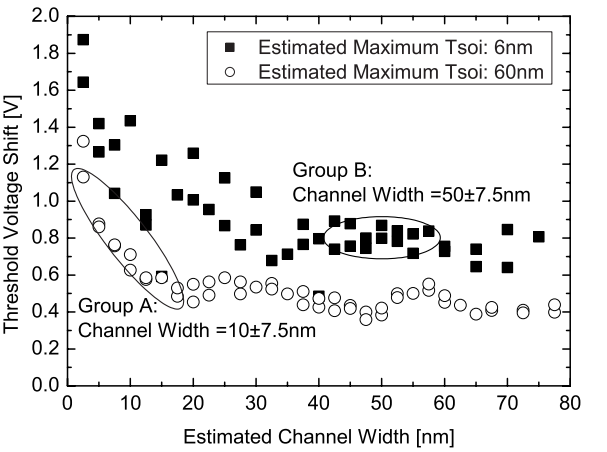

Fig. 5: Channel width dependence of ΔV_{th}. Thin body devices show larger ΔV_{th} than thick body devices when channel width is the same.

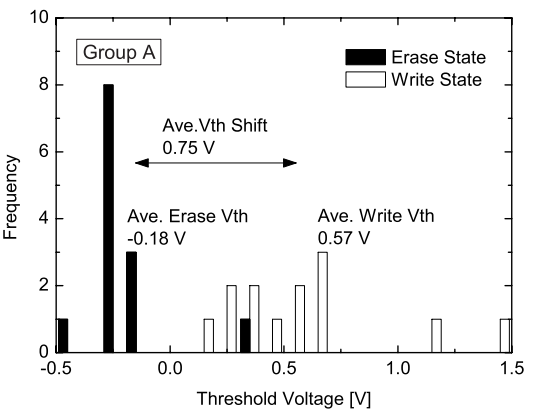

Fig. 6: V_{th} distributions of write and erase states in devices in Group A. Narrow channel devices are sensitive to subtle channel width fluctuations.

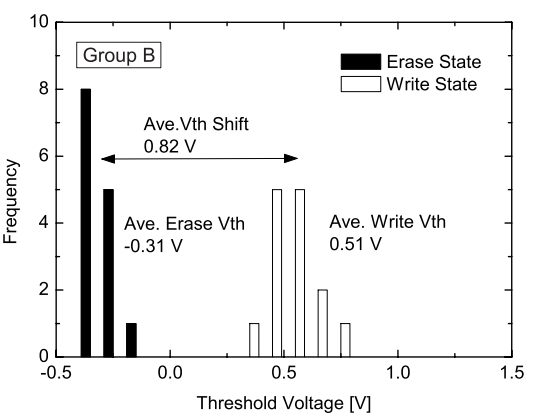

Fig. 7: V_{th} distributions of write and erase states in devices in Group B. Thin body devices show narrow V_{th} distribution and large ΔV_{th} despite relatively wide channel.