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Charge-state control of phosphorus donors in SOI MOSFET

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1. Introduction

Silicon-based nano-electronics recently requires a deep understanding and control of electronic states of individual dopants in MOS structure. For example, threshold-voltage variation due to dopant number fluctuation in nano-transistors is now becoming a serious problem [1]. More positive issue is the establishment of new computer architectures in which charges and/or spins of individual dopants are used [2],[3].

On the other hand, it has already been shown in the 70's that the characteristics of shallow-donor-doped n-channel (i.e., depletion-mode) MOSFETs are influenced by the donor charge states at low temperatures [4]. However, the study, which was aimed at cryogenic-circuits applications, was restricted to conventional bulk MOSFETs and mainly focused on liquid-nitrogen temperature or above.

This paper discusses phosphorus- (P-) doped n-channel SOI MOSFETs from a new standpoint: how we control and monitor charge states of donors in silicon. We will show that SOI-MOSFET characteristics change comprehensively due to neutralization and ionization of P donors.

2. Device structure and fabrication process

SOI MOSFETs with a long and wide ($14 \times 30\ \mu m^2$) channel were fabricated. The SOI layer is (100) boron-doped silicon with nominal resistivity of 14 - 22 Ωcm. Figure 1 shows their schematic top and cross-sectional views. The gate oxide, SOI layer, and buried oxide (BOX) are 87-, 27-, and 400-nm thick, respectively.

Figure 1(b) shows the flow of the fabrication. After the SOI channel was defined, P ions were implanted by 5×10^{12} cm^{-2}. This was followed by thermal activation at 1000˚C. The activation temperature is high enough to make the system achieve thermal equilibrium in terms of P-atom diffusion in the SOI layer and P-atom exchange between the SOI layer and SiO_2/Si interfaces [5]. Thus, we expect that P atoms were uniformly distributed in the SOI layer.

3. Gate-voltage characteristics

Drain current (I_D) vs. gate voltage (V_G) characteristics were investigated at drain voltage of 10 mV with the voltage (V_B) to the substrate (back gate) as a parameter. Figure 2(a) shows the data measured at room temperature. V_B was changed from -12 to +18 V in 2-V step. The I_D-V_G curve at V_B = 0 V (indicated by the bold line) shows that the threshold voltage (V_{TH}) is located in the negative V_G region.

Figure 2(b) plots V_{TH} as a function of V_B, using the data shown in Fig. 2(a). Here, we defined V_{TH} as the gate voltage at which I_D = 10 nA. As a reference, we also plot V_{TH} for a MOSFET that does not contain P atoms. One can see that V_{TH} of the P-doped MOSFET shifts by about 1.3 V in the negative direction from that of the reference MOSFET. This is because of positive charges of ionized P donors. Although P donors have a shallow (~ 44 meV) level beneath the conduction-band edge, most P donors are ionized under subthreshold conditions at room temperature. Upon a uniform spacial distribution of P donors, we estimated P donor density to be 3×10^{11} cm^{-2} from the V_{TH} shift (-1.3 V). This density is one order of magnitude smaller than that of the implanted ions. We should note, however, that such a high degree of dose loss is reasonably consistent with previous studies: P atoms sink into SiO_2/Si interfaces during the thermal activation process and trapped P atoms become electrically inactive [5],[6].

Figure 3 shows the temperature dependence of I_D-V_G curves at V_B = 0 V. One can see that V_{TH} moves in the positive V_G direction in an unusual way as the temperature decreases. A hump (marked by arrows) appears at intermediate temperatures (28 - 60 K). This hump is a typical feature of n-channel MOSFETs with shallow donors at around liquid-nitrogen temperature and caused by a partial carrier freezeout [4]. One can see that the hump rapidly shrinks as the temperature decreases and becomes unobservable at 20 K, suggesting that most P donors were neutralized at 20 K.

Figure 4(a) shows I_D-V_G curves measured at 20 K with V_B as a parameter. One can see that, in contrast to the curves at room temperature [Fig. 2(a)], these curves are not equally spaced. Figure 4(b) plots V_{TH} as a function of V_B. We again plot V_{TH} for a MOSFET without P atoms as a reference.

Figure 4(b) reveals important aspects of low-temperature behavior of P donors in the SOI. First, V_{TH} of the P-doped MOSFET nearly equals to that of the reference MOSFET at around V_B = 0 V. This indicates that most P donors are neutralized at around V_B = 0 V due to carrier freezeout, which is consistent with the temperature dependence (Fig. 3). Secondly, V_{TH} deviation becomes larger as $|V_B|$ becomes larger. This shows that a larger number of P donors becomes ionized as the electric field in the SOI increases. These are evidence that we can control and monitor charge states of donors using SOI MOSFETs. V_{TH} deviation reaches 0.8 V at V_B = + 18 V, but this is still 60 % of that (1.3 V) obtained at room temperature. This imperfect ionization occurs presumably because P donors under and near the electron channel remain neutral. We show in Fig. 5 schematic potential diagrams for three V_B regions to summarize the 20-K results.

4. Summary

Gate-voltage characteristics of a phosphorus-doped n-channel SOI MOSFET have been investigated. It has been shown that, by controlling the voltage to the back gate at 20 K, charge states of P donors can be changed in a controlled way; that is, most donors are neutralized for the back-gate voltage of around 0 V, while major part of donors are ionized for positive or negative voltage.

The present results are the experimental demonstration of systematic control of donor charge states in silicon. We expect that depletion-mode SOI MOSFETs, provided their size is reduced, enable us to monitor, control, and analyze electronic states of individual dopants, which will give us insights for nano-transistors and new computer architectures.

References

[1] J. D. Meindl et al., Science **293**, (2001) 2044.
[2] B. E. Kane, Nature **393**, (1998) 133.
[3] L. C. L. Hollenberg, et al., Phys. Rev. B**69**, (2004) 113301.
[4] F. H. Gaensslen and R. C. Jaeger, Solid-State Electron. **22**, (1979) 423.
[5] Y. Sato et al., J. Electrochem. Soc. **142**, (1995) 660.
[6] H. R. Soleimani, J. Electrochem. Soc. **141**, (1994) 2182.

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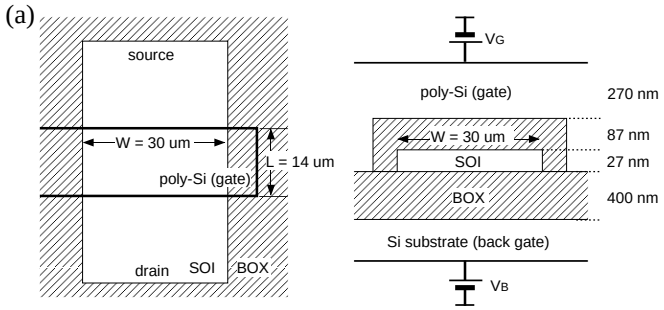

(b)

- **SOI channel definition**
- **Gate oxidation (mask oxidation)**
- **P-ion channel implantation by $5x10^{12}$ cm^{-2} at 55 keV**
- **Thermal activation at 1000˚C in N_2 for 5 min and in O_2 for 8 min**
- **TEOS SiO_2 deposition (as additional gate oxide)**
- **Thermal annealing at 900˚C in N_2 for 30 min**
- **Poly-Si-gate definition**
- **P-ion source/drain implantation (gate mask)**
- **Thermal activation at 900˚C in N_2 for 30 min**

Fig. 1. Top and cross-sectional views of fabricated MOSFETs (a), and a process flow chart (b). In (a), V_G and V_B are voltages to the poly-Si (gate) and to the substrate (back gate), respectively.

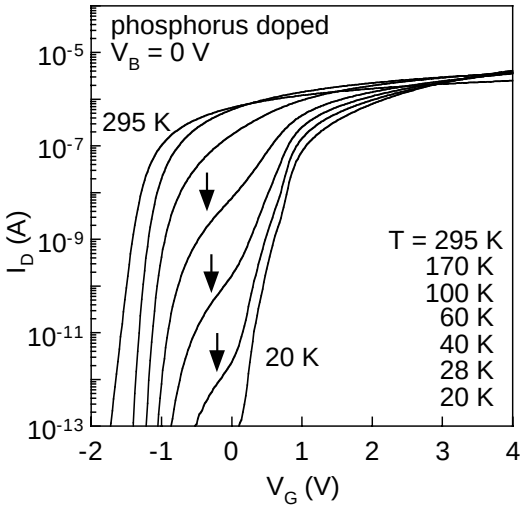

Fig. 3. Temperature dependence of I_D-V_G characteristics of a P-doped MOSFET for V_B = 0 V. The drain voltage is 10 mV. The arrows indicate humps that appear at intermediate temperatures (28 - 60 K).

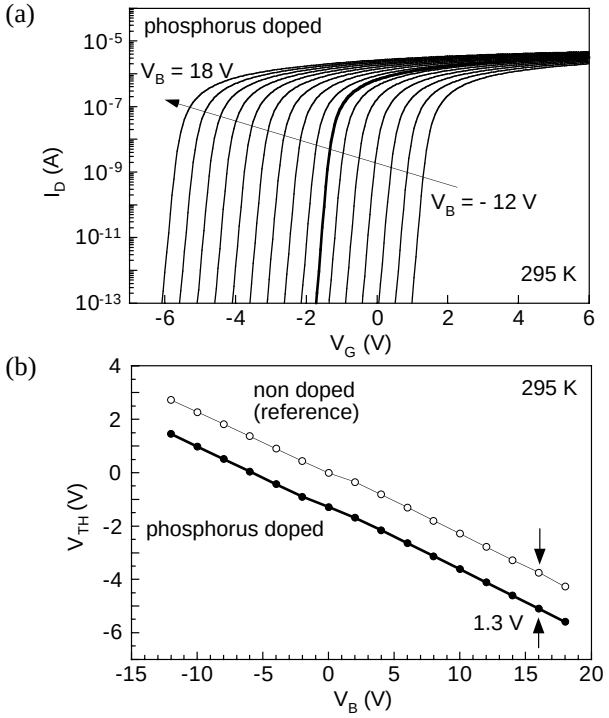

Fig. 2. (a) Room temperature I_D-V_G characteristics of a P-doped MOSFET with back-gate voltage (V_B) as a parameter. V_B is changed from - 12 to + 18 V in 2-V step. The curve for V_B = 0 V is marked by the bold line as a guide. The drain voltage is 10 mV. (b) Threshold voltage (V_{TH}) as a function of V_B. The closed/open circles are the data for the P-doped/non-doped MOSFET. The lines are visual guides.

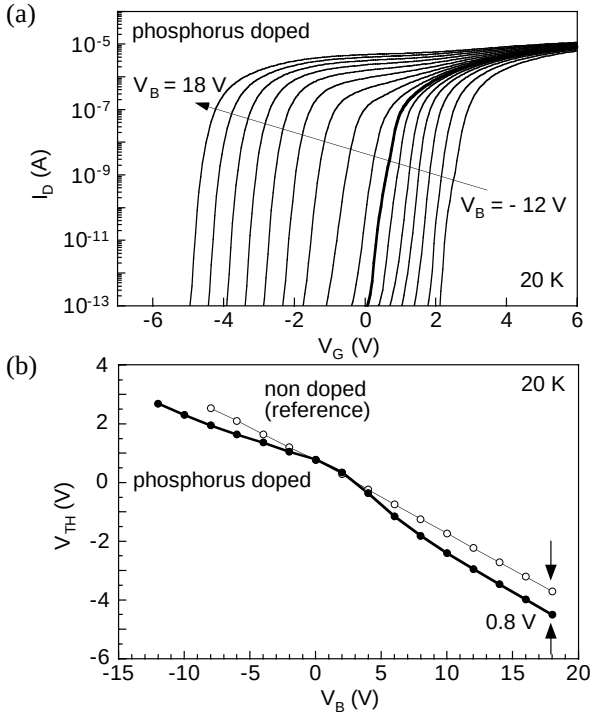

Fig. 4. (a) I_D-V_G characteristics of a P-doped MOSFET, measured at 20 K with back-gate voltage (V_B) as a parameter. V_B is changed from - 12 to + 18 V in 2-V step. The curve for V_B = 0 V is marked by the bold line as a guide. The drain voltage is 10 mV. (b) Threshold voltage (V_{TH}) as a function of V_B. The closed/open circles are the data for the P-doped/non-doped MOSFET. The lines are visual guides.

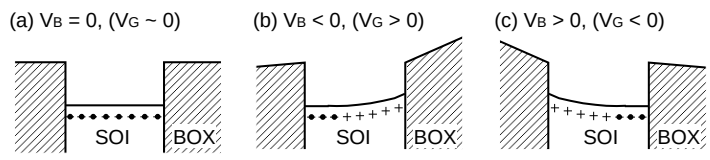

Fig. 5. Schematic illustrations (not based on simulation) of the potential diagram under subthreshold conditions at 20 K for V_B = 0 (a), V_B < 0 (b), and V_B > 0 (c). Closed dots represent electrons trapped in P donors. Crosses represent ionized donors (no electron trapped). In (a), most donors capture an electron and thus the Si conduction-band edge is nearly flat. In (b) and (c), P donors beneath and near the channel capture an electron while those elsewhere are ionized. The Si conduction-band edge is bent due to positive charges.