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Formation of Nanometer-Scale Dislocation Network Sandwiched by Silicon-on-Insulator Layers

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1. Introduction

Formation of regular array of ultrasmall structures is crucial for nanodevices such as multiple single-electron tunneling junctions. Recently, two groups have reported that a network of line defects (screw dislocations) is formed at the bonding interface of Si (001) wafers when the in-plane crystalline direction is misaligned between the wafers [1,2]. Similar dislocation network has been reported for GaAs [3]. It is important that the spacing between the dislocations can be controlled on the nanometer scale by the in-plane misorientation angle (twist angle) [1].

In this paper, thin silicon-on-insulator (SOI) layer containing a nanometer-scale dislocation network is presented, which is fabricated using wafer bonding of a pair of SOI wafers. Such a dislocation network is effective to form a periodic potential laterally in the SOI layer.

2. Fabrication Procedure

Figure 1 schematically shows the fabrication process of SOI layer containing a dislocation network. As the starting wafer, commercially available SOI (UNIBOND) wafers were used, which had a top p-Si (001) layer (~10 ohm cm) of 205 nm and a buried SiO_2 (BOX) layer of 400 nm. First, two wafers were thermally oxidized to reduce the thicknesses of top Si layers (18 nm and 180 nm). After removing the surface oxide in a diluted HF solution, which produces H-terminated surface, the wafers were bonded at room temperature in air. It is noted that the in-plane crystalline direction was intentionally misaligned, leading to the rotational lattice mismatch. Then, the sample was annealed in N_2 (1000°C, 2h) to stabilize the bonding. Finally, the Si substrate and BOX layer (front side) were etched in a KOH solution and a diluted HF solution, respectively [4]. A dislocation network should be embedded at the bonding interface in the top Si layer.

Two samples with the different twist angle (nominally 1° and 5°, accuracy < ±1°) were prepared.

3. Results and Discussion

Transmission electron microscope (TEM) images

Figure 2(a) shows a typical plan-view TEM image taken for the sample with the twist angle of ~1°. A network of dark lines running along <100> directions (period ~ 400 nm) is clearly seen. A plan-view image with a higher magnification is shown in Fig. 2(b). In addition to the network of <100> dark lines, weak line structures (period ~ 60 nm) running along the $[1\bar{1}0]$ direction are seen at the inside of square-shaped regions. The cross-sectional TEM image in Fig. 2(c) also showed the presence of the interface structures with the period of ~60 nm. These two types of periodic structures are probably ascribed to screw dislocations and edge dislocations, which are induced at the bonding interface by the in-plane misorientation and the atomic steps on top Si surfaces before the bonding, respectively [1].

Atomic force microscope (AFM) images

Figure 3 shows a typical AFM image taken on the sample with the twist angle of ~1° after thermal oxidation and oxide removal. The thickness of top Si layer was reduced by 5 nm. As in the case of the TEM observations, a network structure with the period of ~400 nm is seen together with line structures with the period of ~60 nm. As in Fig. 4, these surface corrugations were enhanced with increasing the repetition cycles of the oxidation and oxide removal. This suggests that spatial distribution of lattice strain due to the interface dislocations is present, leading to the spatially modulated oxide growth.

Sheet resistance

Figure 5 shows sheet resistance by four-point probe method on the macroscopic scale. The sheet resistances for the SOI layers containing the dislocations are much lower than that for an as-received SOI without the dislocations. Possible reasons for the lower resistances are (1) conduction through gap states due to the dislocations and (2) band gap narrowing induced by strain around the dislocations.

4. Conclusions

Thin SOI layer containing nanometer-scale dislocation network was shown. The dislocation network would be applicable to form a periodically modulated potential in the lateral direction of SOI layer.

Acknowledgements

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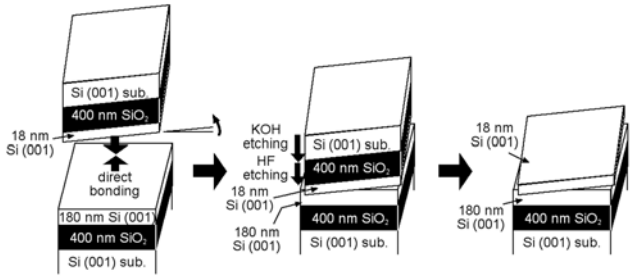

Fig. 1. Fabrication procedure of SOI layer containing a dislocation network.

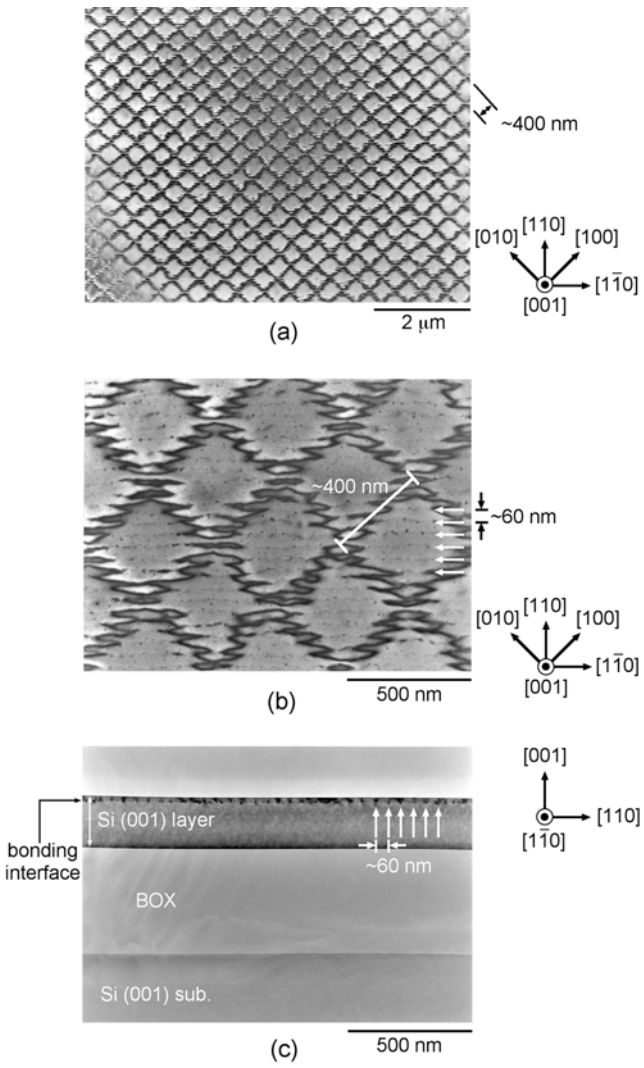

Fig. 2. Typical TEM images taken for a sample with twist angle of ~1°. (a) Plan-view image of the SOI layer, (b) plan-view image with a higher magnification and (c) cross-sectional image.

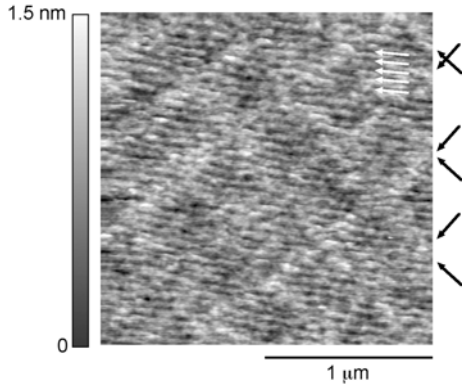

Fig. 3. Typical AFM image taken for a sample with twist angle of ~1°. Using thermal oxidation and oxide removal, the thickness of top Si layer was reduced by ~5 nm (i.e., 13 nm Si on 180 nm Si).

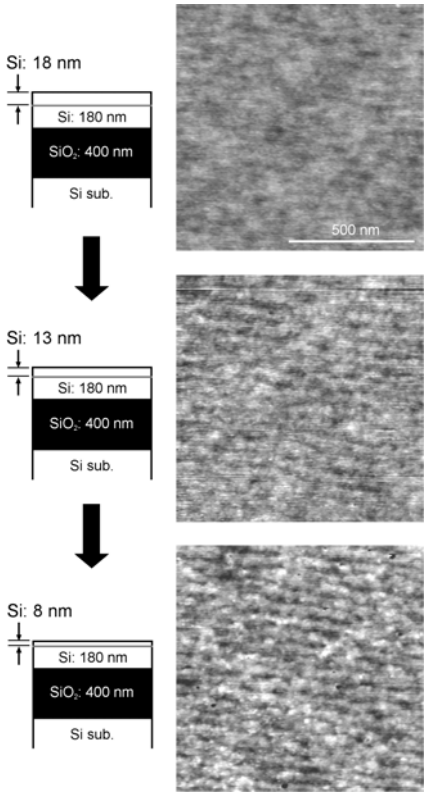

Fig. 4. AFM images showing the change in the surface morphology during the thinning of top Si layer.

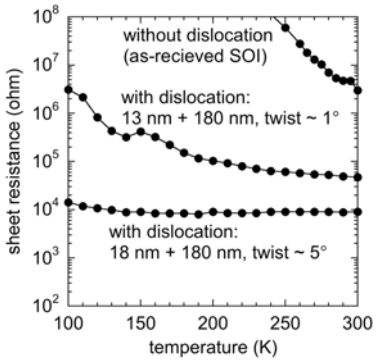

Fig. 5. Sheet resistance versus temperature.