A High S/N Ratio Object Extraction CMOS Image Sensor with Column Parallel Signal Processing

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Abstract
A new CMOS image sensor that has the capabilities of the noise reduction, the column parallel at A/D conversion, the signal processing of object extraction each about 1ms and the video-rate signal output at each 1/60s at the same time is discussed in this paper.

1. Introduction
High quality and high functionality CMOS image sensors have been reported [1-3]. Furthermore, an image sensor with accurate object extraction function is highly demanded in various applications, such as, monitoring FA/ITS and image database construction. The fundamental technology for a high quality and high functionality CMOS image sensor equipped with a real time pre-processing function of highly accurate and high speed object categorizing has been proposed [4]. The pixel size of that sensor, however, was very large because of having A/D converter in each pixel. In this paper, a high functionality CMOS image sensor that has column parallel signal processor for object extraction and high quality video images output is reported.

2. Image Sensor Device and Circuits
The sensor pixel circuit diagram and the timing chart are shown in Fig.1. This unit is composed of a photodiode, a signal readout circuit with noise reduction and sample-hold functions. The reduction of the noise caused by for threshold voltage variations of MOS transistors and thermal reset noise at pixel floating diffusion node is achieved by a combination of the charge transfer operation from the photodiode to the floating diffusion and the sample-hold operation. The operation frequency of the readout is about 1MHz in order to minimize the flicker noise.

The 1-bit circuit diagram of the 4-bit column A/D converter and the timing chart are shown in Fig.2. This unit is composed of a sample-hold circuit with supplying reference voltage circuit, a comparator and a ×2 gain amplifier. After four times pipeline operations, 4-bit digital signal for the object extraction pre-processing is obtained. The 4-bit column parallel A/D conversion operations all of the pixel are carried out at about each 1ms period. The digital signals after A/D conversion are stored in the resistors setting at the side of pixel area and are used in next-stage ALU circuits for extraction.

The size of the sensor pixel circuit is 20µm×20µm and the fill factor of the photodiode is 25% and the A/D converter circuit is 20µm×720µm in designing with 0.35µm 2P3M technology. Fig.3 and 4 shows the plane view of the sensor pixel circuit and the column A/D converter circuit.

3. Real Time Object Extraction Algorithm
The object extraction algorithm is shown in the flow chart of Fig.5. Three feature values for extraction, such as, hue, intensity and texture are selected. The color difference is calculated as 4-bit hue value angle. The color intensity is approximately calculated as 4-bit distance value between the white and the color on the CIE1960 chromaticity diagram as follows;

$$H = \tan^{-1} \frac{G - B}{R - G}$$

$$I = \sqrt{(G - B)^2 + (R - G)^2}$$

where H is color difference and I is color intensity. Because it is difficult to implement this equation directly into the hardware circuit, the calculation of Tan\(^{-1}\) is carried out by simple three step conditional branch operations and I are simplified as follows; $I = \max\{|G - B|, |R - G|\}$.

The texture is represented as 4-bit difference value between maximum and minimum intensities in a referred pixel and its neighboring eight pixels. By this processing, the luminance variation in the 3×3 pixels block is converted to the space frequency.

The object extraction operations are performed at every sub-frame period of about 1msec by the extracted feature values that is the color difference, the color intensity and the texture.

The 4-bit category number for each pixel and the 8bit analog video signal are outputted from the sensor every 1000frame/sec and 60 frame/sec, respectively. Finally, the motion is calculated as 1-bit value from succeeding sub-frame categorized data. When the extraction data are differ from the next sub-frame extraction data, the object sensing by the pixel are regarded as the motion object.

Fig.6 shows the result of the object extraction by this algorithm. Fig.7 shows the plan view of the sensor chip. Fig.8 shows the specifications of the sensor chip.

4. Conclusion
A high S/N ratio object extraction CMOS image sensor with column parallel signal processing is developed. The image sensor can be utilized in various image processing applications.

Reference
Fig. 1: The sensor pixel circuit diagram and the timing chart

Fig. 2: The 1-bit circuit diagram of the 4-bit column A/D converter and the timing chart

Fig. 3: The plan view of the sensor pixel circuit

Fig. 4: The plan view of the column A/D converter circuit

Fig. 5: The object extraction algorithm flow chart

Fig. 6: The result of the object extraction

Fig. 7: The plan view of the sensor chip

Fig. 8: The specifications of the sensor chip