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An Analog Edge-Filtering Processor Employing Only-Nearest-Neighbor Interconnects

Yusuke Nakashita, Yoshio Mita* and Tadashi Shibata

Department of Frontier Informatics, School of Frontier Sciences, The University of Tokyo
5-1-5 Kashiwanoha, Kashiwa-shi, Chiba, 277-8561, Japan
Phone: +81-4-7136-3853 FAX: +81-4-7136-3855 E-mail: yusuke@else.k.u-tokyo.ac.jp
*Department of Electrical Engineering, School of Engineering, The University of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-8656, Japan

1. Introduction

Edge detection is an essential operation in various image processing algorithms, particularly in image recognition. In fact, biological systems utilize the edge information for recognizing objects. For human-like image recognition, we have developed an edge-based algorithm called Projected Principle Edge Distribution (PPED) and verified its applicability to hand-written characteristics recognition [1], medical X-ray analysis [2], and human face detection [3]. PPED uses four-direction edges: +45degree, -45degree, vertical, and horizontal. The edge detection, however, is computationally very expensive, and direct hardware implementation is mandatory for real time processing. In addition, for compact implementation as well as for low power operation, an analog image filtering smart sensor is a promising approach.

On the other hand, when we implement edge filters on hardware, we encounter a difficulty which we call "interconnection explosion." As shown in Fig. 1, extremely complicated multi-level interconnects are required if each pixel sensor is connected to its nearest-neighbor and next-nearest-neighbor pixels. It is almost impossible to implement with current technologies.

In this paper, an analog image filtering smart sensor for real-time edge detection is presented. We have developed the "Only-Nearest-Neighbor Interconnects" architecture, in which each processing element is connected to only nearest-neighbor (N. N.) pixels by interconnects. However, each processing element can gather from its N. N. and next N. N. pixels all data necessary for edge filtering processing. With this architecture, we can detect four direction edges using simple circuits based on the floating-gate MOS technology. A test chip was designed and fabricated in a 0.35-μm double-poly, triple-metal CMOS technology, and the experimental results of the edge detection from gray-scale images are presented using the fabricated test chip.

2. Edge Detecting Algorithm

In order to achieve a simple interconnection, we have proposed a new architecture named "Only-Nearest-Neighbor Interconnects" shown in Fig. 2(a). The notable feature of this architecture is that the photo-diodes (input devises) are staggered with respect to the array of processing elements (PE's). This is in contrast to the conventional architecture in which a photo diode (PD) is placed in each processing element (PE) as shown in Fig. 2(b).

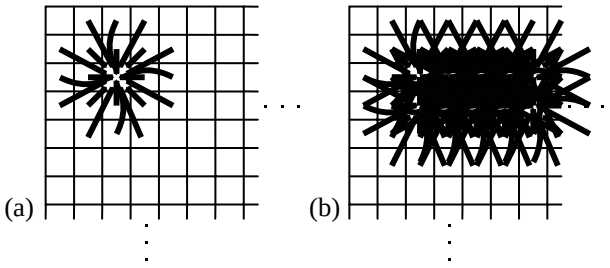


Fig. 1. (a) Interconnects from nearest neighbor (N. N.) and next N. N. pixels to a single pixel at the center. (b) N. N. and next N. N. interconnects for pixels in the two rows, an illustrative example of "interconnection explosion."

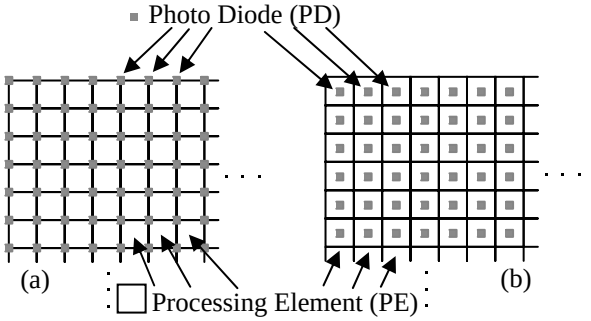
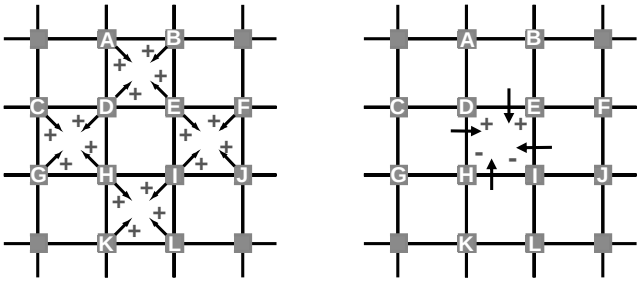


Fig. 2. Only-Nearest-Neighbor Interconnects (a), in comparison with conventional image-filtering architecture (b).



(a) First step **(b) Second step**

Fig. 3. Edge detection process. (+45degree)

Then, we show how to detect edges in the "Only-Nearest-Neighbor Interconnects" architecture.

1) First, each PE gathers luminance data from four PD's locating at its corners and takes the sum of these data (Fig. 3(a)).

2) Second, the data are sent to nearest neighbor PE's and subtraction is carried out (Fig. 3(b)). (Subtract operation is illustrated in Fig. 6.)

Then, the result obtained at the center PE is shown below. (The alphabets indicate the PD outputs in Fig. 3.)

$$(A+B+D+E)+(C+D+G+H)-(E+F+I+J)-(H+I+K+L)$$
$$=A+B+C+2D+G-F-2I-J-K-L$$

This computation is equivalent to the filtering operation using the kernel of Fig. 4(a). Other kernel operations can be performed in similar ways. The kernel in Fig. 4(c), for instance, is achieved using similar two-step arithmetic operations; in which the sum operation in the first step is changed to subtraction in some PE's as shown below.

$$(A+B+D+E)+(C+D-G-H)-(-E-F+I+J)-(H+I+K+L)$$
$$=A+B+C+2D+2E+F-G-2H-2I-J-K-L$$

0	1	1	0
1	2	0	-1
1	0	-2	-1
0	-1	-1	0

(a) +45

0	1	1	0
-1	0	2	1
-1	-2	0	1
0	-1	-1	0

(b) -45

0	1	1	0
1	2	2	1
-1	-2	-2	-1
0	-1	-1	0

(c) horizontal

0	1	-1	0
1	2	-2	-1
1	2	-2	-1
0	1	-1	0

(d) vertical

Fig. 4. Edge filtering kernels obtained by "Only-Nearest-Neighbor" architecture.

3. Circuit Configuration

In this architecture, we need only two arithmetic operations, i.e., the sum of four numbers and the subtraction. They are achieved easily using the floating-gate MOS technology. Fig. 5 shows the adder circuit. Fig.6 shows the subtraction circuit.

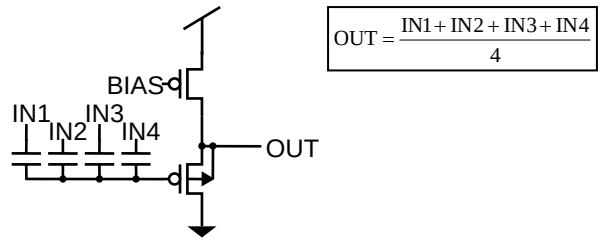


Fig. 5. Adder circuit using floating-gate MOS technology.

4. Measurement Results

A test chip employing the "Only-Nearest-Neighbor Interconnects" architecture was designed and fabricated in a 0.35-μm CMOS technology. Fig. 7 shows the layout. The test chip was designed to verify the concept and an array of 7x7 PE's was fabricated. Photo diodes were not included and 8x8 input nodes were provided to receive image data from outside.

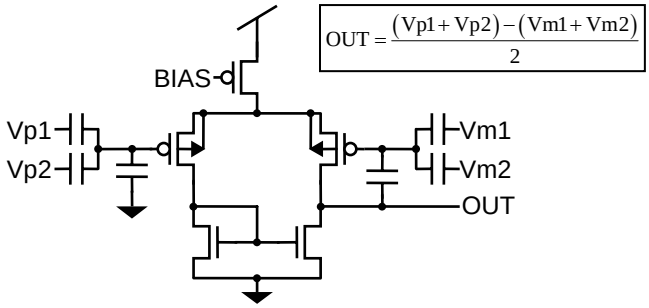
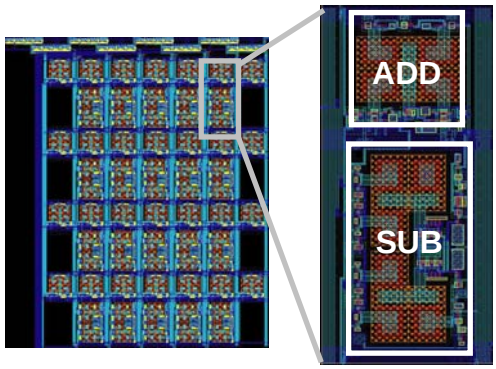


Fig. 6. Subtraction circuit.



(a) 7x7 PE array **(b) Single PE circuit**

Fig. 7. Layouts of test circuit.

The measurement results are demonstrated in Fig. 8. Fig. 8(a) is an input original image that is given to the test chip as multiple 8x8-pixel data. Fig. 8(b) is the output image obtained from the chip. Fig. 8(c) is the simulation results on C-language program using kernel shown in Fig. 4(a).

Acknowledgements

The VLSI chip in the paper was fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

References

[1] M. Yagi, M. Adachi, and T. Shibata, in *Proc. 10th European Signal Processing Conference (EUSIPCO 2000)*, Tampere, Finland, Sept, 2000, p.729.

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(a) Input image

(b) Measurement results

(c) Simulation Results

Fig. 8. Measurement results from the fabricated test chip.