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CMOS-process-based ultra high density Flash Memory Cell and Array Architecture

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1. Introduction

The industry standard EEPROM/flash memory cells are largely based on multi-gated structure. Due to a high demand in embedded nonvolatile memory (NVM) for system integration on a chip, single-poly EEPROM/flash cells [1]–[3] become an active research topic in recent years. Conventional cells requires a large area N-Well or P-Well as floating gate coupling node, the bit sizes are often too large for high density NVM applications. A single-poly EEPROM cell [4] with a channel hot hole for programming and channel hot electron for erasing schemes were proposed by our group. In this work, we present a fully CMOS logic process compatible flash cell with common select gate and floating node structure with reduced cell size. A feature-sized n-MOSFET per non-volatile memory bit is successfully demonstrated and the CMOS-process-based flash cell size can be as small as multi-gated flash memory.

2. Cell Structure and Array Architecture

The novel flash memory cells arranged are shown in Fig. 1(a), in the same word line, ex. WL0, array page, every cell composed of two serial N-channel MOSFET, an identical select transistor (SG) and a floating gate transistor (FG) via a common floating N^+ node, X. Area per bit under the standard logic process design rule is about $24F^2$ as shown in the cell layout in Fig. 1(b). The memory cell area is the smallest among the reported CMOS-process-based non-volatile memory cells. The memory devices and the corresponding dummy memory devices are fabricated by 0.35μm standard logic single-poly CMOS technology. The oxide thickness under the select gate and the floating gate is 7.5nm. The sample devices measured have transistor width, select transistor gate length, floating gate length designed as 5μm, 0.35μm, and 0.35μm respectively.

3. Operation Principles and Experiments Results

Table 1 lists the operating conditions of the cell. A cell can be programmed and erased by channel hot hole and channel hot election injection respectively, same as the EEPROM operation reported in our previous work [4]. Fig. 2 shows I_{FG} measured on the dummy cell with respect to sweeping V_{FG}. By choosing the proper select gate voltage, programming and erasing the cell can be achieved.

The novel flash memory array operates in page programming, erasing, and reading modes. The selected word line (WL) and its corresponding floating storage gates are connected via a common N^+ diffusion line. The SPICE simulated floating gate voltage states are shown in Fig. 3, more than 100 cells can be connected in the same page without affecting their operation characteristics. The 6V bit line voltage programming measurement results are shown in Fig. 4. Read current is measured under the conditions of V_{SG}=3V, V_{SL}=3V, and V_{PW}=V_{BL}=0V. While M1 and M2 are at the programmed states, the programming characteristics of M3 and M4 in the inset of Fig. 4 show a slightly disturbance. This problem can be alleviated by lower the operating bit line voltage to 5.5V as shown in Fig. 5. Select gate controlled erasing characteristics are shown in Fig. 6 and Fig. 7. To lower the erasing state read current, higher floating gate voltage coupled by source line biasing is obtained in Fig. 7. The read disturbance measurement results shown in Fig. 8 demonstrate visually no read disturbance effect in the new cell. The endurance characteristics of the flash cells are shown in Fig. 9. The read current window exhibits only minimal narrowing up to 10^5 program/erase cycles. The cell's retention characteristics after 10^5 cycling stress in Fig. 10 shows 10 years reliability is obtainable.

4. Conclusions

A high density flash memory cell fabricated by standard CMOS logic process and operated by 6V voltage has been introduced. With novel operation principles and array architecture, the smallest bit area of a CMOS-process-based flash memory cell is proposed. The floating gates in an array page are arranged by sharing one select gate and a common floating node. Operated by select-gate-controlled channel hot hole programming and channel hot electron erasing, one n-MOSFET per non-volatile memory bit has been successfully demonstrated. 10^5 cycling endurance and 10 years excellent retention characteristics of this cell are observed. This new technology is a paradigm change in embedded nonvolatile memory applications.

Acknowledgement

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References

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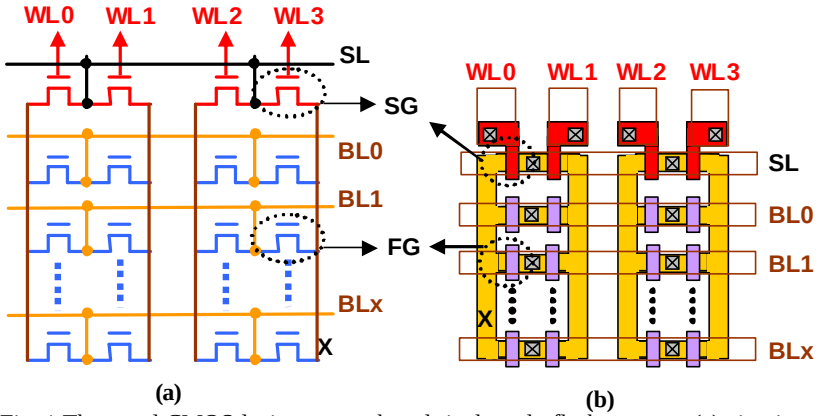

Fig. 1 The novel CMOS-logic-process-based single-poly flash memory (a) circuit schematic and (b) layout of the array architecture

	BLx		WLx		SL
Program	Select	Unselect	Select	Unselect	0V
	6V	Float	4V	0V	
Read	0V		3V	0V	3V
Erase	6V		2V		1V

Table 1. Typical operation conditions

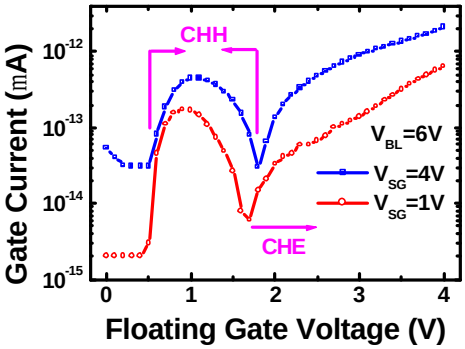

Fig. 2 The floating gate currents corresponding V_{SG}=1V and V_{SG}=4V are measured by dummy cells.

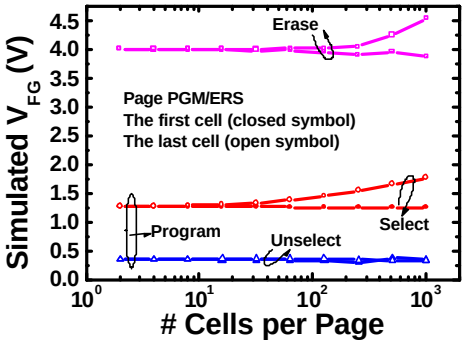

Fig. 3 The tolerance of PGM/ERS simulations show more than 100 cells can be strung in a page.

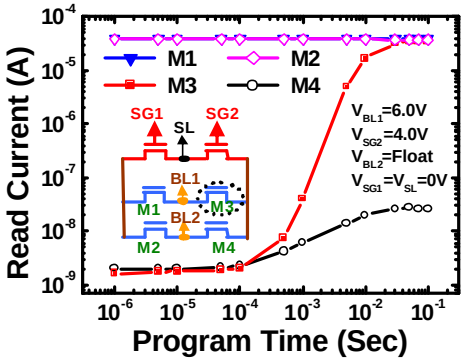

Fig. 4 Slight disturbance is shown in the 6V programming operation.

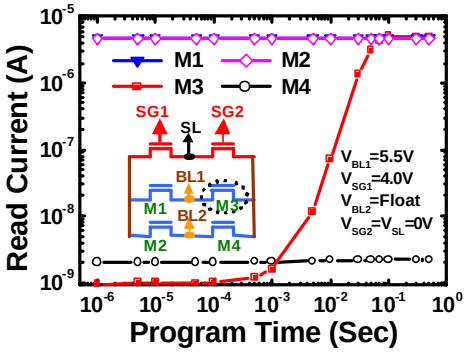

Fig. 5 The programming disturbance of M4 can be alleviated by 5.5V bit line operation.

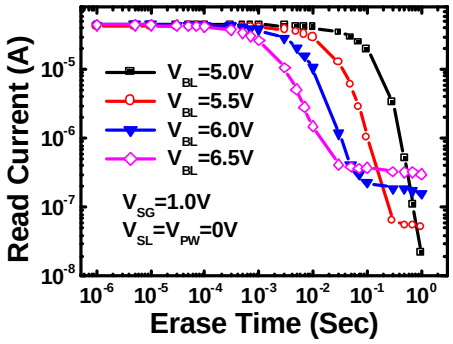

Fig. 6 Channel hot election erasing characteristics are measured by 5~ 6.5V bit line voltages.

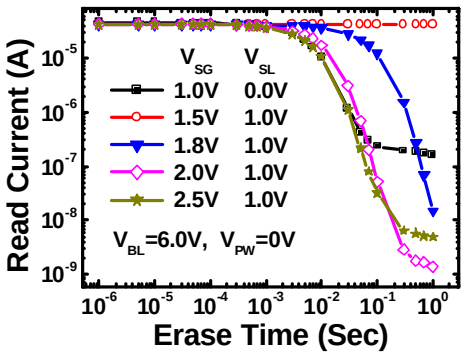

Fig. 7 The higher floating gate voltage coupled by source line biasing make lower erasing state and read current.

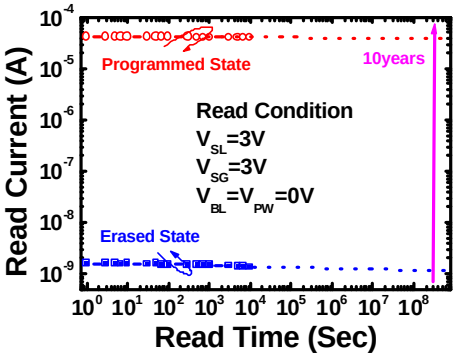

Fig. 8 There is almost no effect on the storied charge of the floating gate at the read conditions.

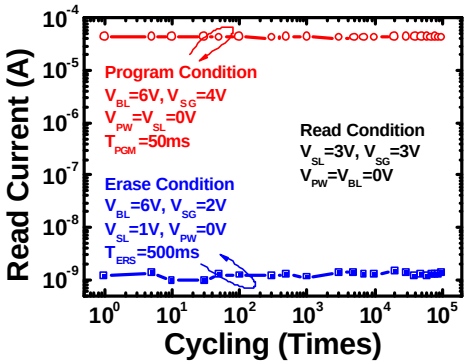

Fig. 9 Endurance experiment in a single cell is up to 10^5 cycles.

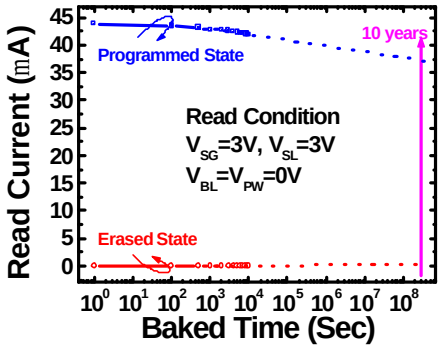

Fig. 10 The flash cell's 150°C high temperature data retention characteristics after 10^5 cycling stress.