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Fast-lock and Low-power DLL with Super-short Cyclic Delay Line

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1. Introduction

In recent years, the power consumption of application processors and memories for cellular phones has been progressively lowered. With this situation, it has become increasingly important to reduce the electric power of the whole system, i.e., (1) supply/stop the clock in a shorts time units, and (2) operate over a large frequency range to respond to various frequency operations that require optimal decision to be made for various system demands. It has also become important to have (3) the high portability of system which can be used for another product or another process. For the above (1), the circuit system which can be fast locked, furthermore for (2) the circuit system which can respond to the frequency range which reaches 5-10 times, without making the number of gates or circuit electric power increase compared with the case of fixed frequency operation, and for (3), the all digital system which eliminated the analog circuit with a strong potential for addiction of a process or manufacture line is needed. In response to the requirements described above, we report a new system in which the fast-lock advantage and the wide operating frequency range are achieved by featuring the super short cyclic delay line even with the reduced number of gates and power consumption.

2. Conventional Circuit

A SMD[1] (synchronous mirror delay) circuit (Fig. 1) is used as a fast-locking DLL. It consists of an FDA (forward delay array), an MCC (mirror control circuit), a BDA (backward delay array), a driver, and a dummy delay circuit with the same delay time as the driver. Phase synchronization is performed by comparing the phase of the Ext.CLK1 (external clock 1 (t_{ck})) input to the FDA through the dummy delay circuit with the Ext.CLK1 input into the MCC and the output stage (t_{ck} - t_{dummy}) is determined to be where the coincidence signal from the MCC is output. Ext.CLK2 (t_{ck}) is inputted in the reverse direction of the FDA from the same position as that detected in the FDA and it outputs (t_{ck} - t_{dummy} + t_{drv}) through a driver (t_{drv}). The phases of the external clock and the internal clock are synchronized by designing the dummy delay circuit such that it has the same delay as the driver (t_{dummy} = t_{drv}). This circuit system makes the delay stages and PD parallel, and two-cycle lock is achieved by performing phase comparisons all at once. However, by raising the resolution of one stage of the delay stage for a high and wide range of operating frequencies, the resulting large increase in the number of delay stages poses several problems. For example, the number of gates and power consumption are increased. In particular, the circuit area which is proportional to the number of delay stages, such as the MCC, FDA, and BDA, is increased with the increasing number of delay stages and power consumption also increases. To solve this problem, the authors have developed a cyclic-delay-type DLL circuit that uses a super-short delay line.

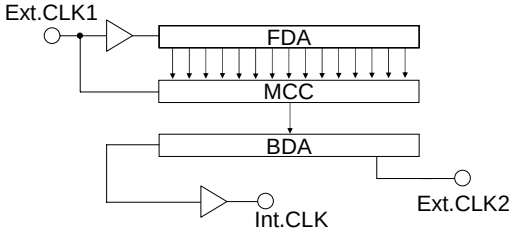

Fig. 1: Synchronous Mirror Delay

3. New DLL

3.1 Circuit architecture

The cyclic-delay-type DLL expands operating frequency without increasing the number of gates or power consumption and inherits a two-cycle lock feature like SMD. There is a block diagram of the DLL in Fig. 2. This new circuit architecture can create a delay time longer than the actual delay line by using a super-short delay line and passing the signal two or more times. The clock is inputted into the PD (phase detector) and inputted into the MDL (measure delay line) through the dummy delay circuit and a selector switch. This dummy delay circuit is dummy of the driver, OSEL (output selector), and OCTL (output control circuit). In the delay-measurement part, the MDL's CNT (MDL's counter) counts and records the number of times the signal passes through the MDL until the lock signal is outputted from the LGC (lock-signal generation circuit).

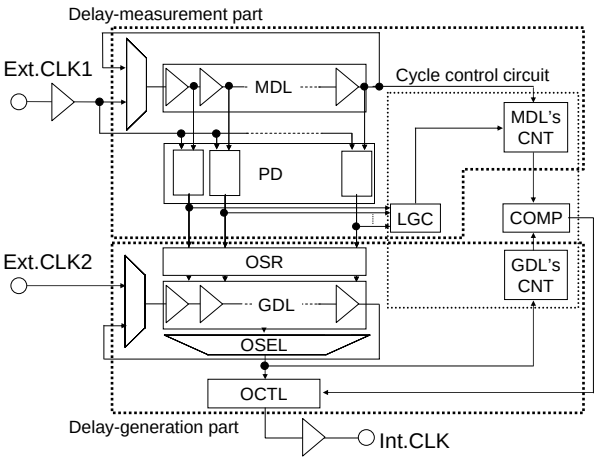

Fig. 2: New DLL with cyclic delay line

Furthermore, the OSR (output stage resistor) records the output stage by using this lock signal. Ext. CLK2 (External clock2) is fed into the GDL (generation delay line) and passes through the same number of times as counted by the MDL's CNT. The delay clock is then outputted from the delay stage as specified by the OSR. The MDL's CNT, COMP, GDL's CNT, and LGC are collectively labeled CCC (cycle control circuit). The condition described below is necessary for phase synchronization to be executed properly.

3.2 Minimum number of delay stages

The delay stages should be reduced to minimum to solve the problem of number of gates and power consumption. The factor that determines the minimum number of delay stages for the delay line is the sum of the GDL's CNT and COMP (comparator). In order to pass through the GDL the same number of times as counted by the MDL's CNT, the circuit operation of GDL's CNT and COMP must be completed where a clock can be outputted before a clock is outputted from the OSEL. Given the delay time for one stage of the delay stage, t_d, the delay time for the GDL's CNT, t_{cnt}, and the delay time for the COMP, t_{comp}, a conditional expression of the number of delay stages, n, can be formed as follows:

$$n > \frac{t_{cnt} + t_{comp}}{t_d}.$$

4. Evaluation results

The number of delay stages, number of gates, and power consumption of the developed DLL were evaluated by applying it to the phase synchronous circuit of the bus interface between an application processor and a DDR-SDRAM in a typical cellular phone. This circuit was fabricated with the 0.13-μm process, and its supply voltage was set to 1.2 V under an expanded operational-frequency range of 20 to 150 MHz against SMD.

4.1 Delay stages

The minimum number of delay stages was evaluated with HSpice as described in section 3.2. The simulation revealed that if the frequency range was expanded using a

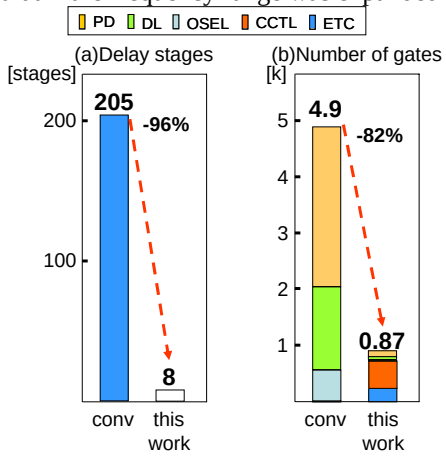

Fig. 3: Estimated delay stages and number of gates

Table 1: Number of gates

	Conventional	New(ratio to conventional)
PD	2829	110(0.04)
Delay line	1476	50(0.03)
OSEL	575	22(0.04)
CCC	-	493(-)
Rest	20	292(14.6)
Total	4900	867(0.18)

Table 2: Power consumption

	Conventional	New (ratio to conventional)
PD	0.71mW	0.08mW(0.11)
Delay line	1.00mW	0.30mW(0.30)
OSEL	0.02mW	0.04mW(2.00)
CCC	-	0.18mW(-)
Rest	0.06mW	0.47mW(7.83)
Total	1.79mW	1.07mW(0.60)

conventional circuit, the number of delay stages would have to be no less than 205 (Fig. 3-(a)). However, if our new system were used, it would significantly be reduced to 8 stages. That is, this new system can reduce it by 96%.

4.2 Number of gates

Owing to a super-short delay line of eight stages, the number of gates can be reduced to about 18% of that in the conventional circuit, as we can see from Fig. 3-(b) and Table 1. In particular, the proposed DLL makes it possible to sharply reduce it in the PD and delay line, which become a bottleneck in the SMD when the frequency range is expanded.

4.3 Power consumption

Compared with the power consumed by the conventional system, that of the system we developed was reduced by 40%, as we can see from Table 2. This was because the power consumption reduction afforded by the lower number of delay stages and PDs exceeded the increase in power caused by the additional CCC, OSR and so on.

5. Conclusion

A fast-lock cyclic-delay-type DLL with super-short delay line was developed, featuring an expanded operation frequency range of 20 to 150 MHz and a sharply reduced number of gates and power consumption. Compared with the conventional circuit, the developed DLL features 82% fewer gates (867) and 40% lower power consumption (1.07 mW) at 150 MHz operation frequency. The circuit operation verified through simulation proved that this DLL could meet the low power demands of future mobile devices.

References

[1] T. Saeki et al., IEEE Journal of Solid-state Circuits, Vol. 31, No. 11, November 1996, pp1656-1668