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18 GHz Operation of an 8-bit Microprocessor Based on a Single-Flux-Quantum LSI Technology

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1. Introduction

Single-Flux-Quantum (SFQ) logic circuits utilize high-speed propagation of an SFQ voltage pulse in a superconducting circuit as a logical bit information [1]. Presence (absence) of an SFQ voltage pulse during clock periods represents a logical "1" ("0"). SFQ logic circuits have the following excellent features as a digital logic circuit:

i) Very high-speed operation. Clock frequencies beyond 700 GHz have been demonstrated [2].
ii) Extremely low power. Power consumption of an SFQ gate is about 10^{-7} W at 100 GHz.
iii) Compact and high-throughput interconnection using passive transmission lines (PTLs) [3]. Ballistic propagation of an SFQ voltage pulse with dissipation-free and dispersion-free is possible at the speed of light using submicron-wide superconductive PTLs.

All these features make this technology attractive for high-end digital applications, where the 4.2K cooling cost is relatively ignored.

We have been developing SFQ microprocessors named CORE1 in order to study the feasibility of a high-end SFQ microprocessor and figure out the problem in complex digital system design. Just recently we have successfully demonstrated the complete operation of our prototype microprocessor, CORE1α5 [4]. CORE1α5 is the first SFQ microprocessor operating at 15.2 GHz with power consumption of 1.6 mW. In that design a Josephson transmission line (JTL), which is a simple SFQ circuit element just propagating an SFQ pulse, is used for the connection between all circuit blocks.

The purpose of this study is to improve the performance of the CORE1 microprocessor by employing PTLs between circuit blocks. Utilization of PTLs will help to decrease the propagation delay between circuit blocks, give the flexibility of a floor plan in a chip design, and reduce the power consumption of the system. A system clock generator, as well as a local clock generator is also integrated on a chip to perform the high-speed on-chip test. In this paper we will show the improved design of the CORE1 microprocessor using PTLs and its successful demonstration at 18 GHz.

2. Design of SFQ Microprocessor, CORE1α6

Figure 1 is a microarchitecture of our new version of SFQ microprocessors, CORE1α6. CORE1α6 is an 8-bit microprocessor based on the bit-serial architecture, where one 8-bit word is transferred serially between each circuit block. It is composed of a 1-bit ALU, three 8-bit registers (Reg0, Reg1 and IR), a program counter (PC), data switches (DS1 and DS2) and a controller. It executes seven instructions including halt, add, load, store, skip if zero, jump and move operations. Compared with the previous microarchitecture [4], DS2 is added to adjust the data format so as to fit an SFQ memory [5]. (In this version the SFQ memory is not implemented, but shift registers are included instead of it, which is shown in Fig.1 as ST_SR and LD_SR.) The number of system clock cycle per instruction is also changed from six to five in the new design. This is due to the reduction of propagation delay between circuit blocks by using PTLs. For example, the propagation delay between DS1 and IR is reduced from 400 ps to 34 ps by PTL.

The CORE1α6 microprocessor was implemented by using the CONNECT cell library [6] and the NEC standard Nb process [7]. Figure 2 shows a photograph of a

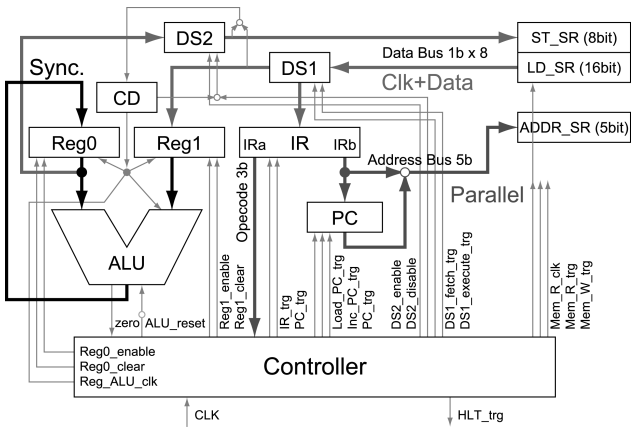

Fig. 1 A microarchitecture of CORE1α6.

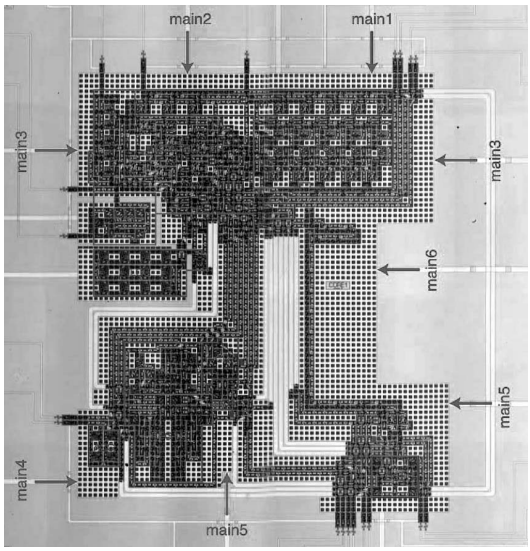

Fig. 2 A photograph of a CORE1α6 chip. A circuit size is 3.44 mm x 3.88 mm.

CORE1α6 chip, which is composed of 6319 Josephson junctions. In the photograph, white lines correspond to PTLs, whose impedance, line width and propagation delay are 2 Ω, 34 μm, and 8.6 ps/mm, respectively.

3. Test results

Functionality of CORE1α6 was tested at high speed by using the on-chip high-speed test system. Frequencies of local and system clock generators are 16 GHz and 1 GHz, respectively, at the design point. The former determines the frequency of bit-serial operations and the latter corresponds to the frequency of the system cycle. We have confirmed correct operations of the CORE1α6 for the execution of all instructions. Figure 3 shows one example of test results, where successive operations of load, add and store instructions are tested. We have also examined the operating range of the microprocessor for the bias current changes at different local clock frequencies. The results are shown in Fig. 4. It is found that the maximum local clock frequency is 18 GHz. The maximum system clock frequency is also examined and found to be 1.2 GHz, which corresponds to the performance of 240 million instructions per second (MIPS). The total power consumption of CORE1α6 microprocessor including the on-chip high-speed test system is 2.1 mW.

4. Conclusions

We have improved the performance of a prototype 8-bit SFQ microprocessor by employing superconductive passive transmission lines. Its complete operation has been demonstrated at high speed. Its maximum local clock frequency and system clock frequency were found to be 18 GHz and 1.2 GHz, respectively.

Acknowledgements

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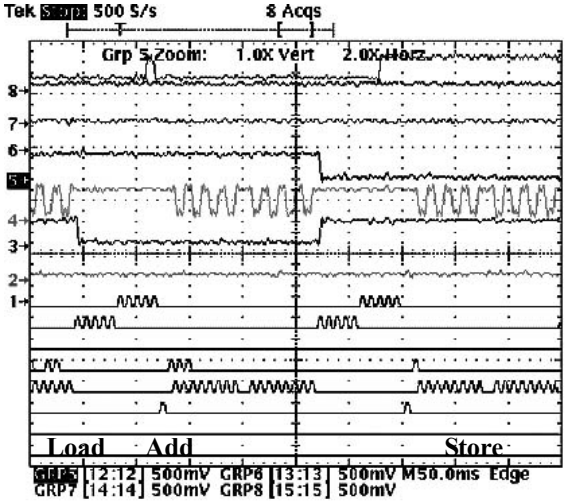

Fig. 3 A test result of load, add and store operation.

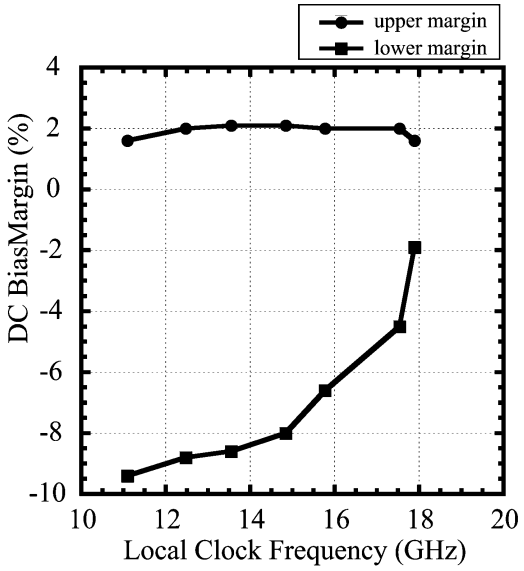

Fig. 4 The dependence of the operating range of CORE1α6 for the bias current changes on local clock frequency. The area surrounded by upper and lower bias margins indicates the operational region. The 0% value corresponds to the design point.

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