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High-Speed Digital Systems by Hybridization of CMOS and Single-Flux-Quantum Logic Circuits

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1. Introduction

Hybridization of recently developed single-flux-quantum (SFQ) logic circuits [1] and well-established CMOS circuits has a possibility to open a new field of high-performance digital systems, where both of advantages of two technologies, very high speed and low power consumption in the SFQ circuits and very high density of CMOS digital circuits, are utilized effectively. Besides, operation of CMOS devices at cryogenic temperatures causes an improvement in device characteristics: enhancement of the device speed and reduction of the leakage current are expected.

Examples of the hybrid system are a hybrid analog-to-digital converter (ADC) [2] and a hybrid SFQ/CMOS memory [3,4]. In the hybrid ADC, a semiconductor ΣΔ modulator in a ΣΔ ADC system is replaced with a high-speed SFQ ΣΔ modulator, by which an over sampling rate beyond 20 GHz can be obtained. The hybrid SFQ/CMOS memory employs high-density semiconductor memory cells and highly-sensitive Josephson sense circuits to get sub-nanosecond access time.

There are several important technologies to realize the SFQ/CMOS hybrid system; these include characterizations of CMOS devices at cryogenic temperatures, a high-speed interface between SFQ and CMOS circuits and an SFQ/CMOS multi-chip module. In this paper, we will show the recent progress in the hybridization technologies. The main concern here is 4.2 K CMOS device characterizations and the development of the SFQ/CMOS hybrid memory.

2. CMOS Device Characterizations at 4.2 K

Operating MOS devices at 4.2 K improves device performance by a factor of about 30-40% in short-channel MOS devices. Increase of the carrier mobility enlarges their current driving ability and the freeze-out of carriers decreases the parasitic capacitance. In order to perform accurate simulation of low-temperature CMOS circuits, characterizations and modeling of CMOS devices at 4.2 K are necessary. CMOS devices examined in this study have been fabricated by using the 0.35 μm Rohm process and the 0.18 μm Hitachi CMOS process.

Figure 1 shows I-V characteristics of a 0.35 μm nMOS device fabricated by Rhom Corporation. We have modified parameters of the room temperature BSIM3 device model [5] so as to fit calculated data to experimental data. One can see that quite good agreement is obtained, except that a small kink is observed in the experimental data. This is due to a hot-carrier effect in the drain region. The junction capacitances between the drain (or source) and the substrate have been also measured at low temperatures in order to simulate the transient characteristics of CMOS circuits. An 80-90% reduction in the drain-substrate capacitance is observed due to the carrier freeze-out at 4.2 K. Based on these data, we have made a set of device model parameters for low temperatures. The propagation delays of CMOS inverters also were measured at 4.2 K and these data were compared with simulation results. The experimental results indicate that 30-40% speedup is obtained at 4.2 K compared with those at room temperature, which coincides well with the simulation results using the low-temperature device model.

3. SFQ/CMOS Hybrid Memory

An SFQ/CMOS hybrid memory operating at 4.2 K has following remarkable features: (i) High-speed CMOS operation at 4.2 K; (ii) Nonvolatile memory operation due to vanishing leakage current at low temperatures; (iii) Nondestructive memory operation by using a three-transistor DRAM cell; (iv) High-speed and low-power operation by using Josephson sense circuits.

Figure 2 (a) shows the architecture of the 64 kb SFQ/CMOS hybrid memory. It consists of an SFQ-CMOS interface, a CMOS decoder, a three-transistor memory cell array and a Josephson current-sense circuit. A circuit schematic of the three-transistor memory cell is shown in Fig. 2 (b). It is a DRAM cell, where charge is stored in a node x.

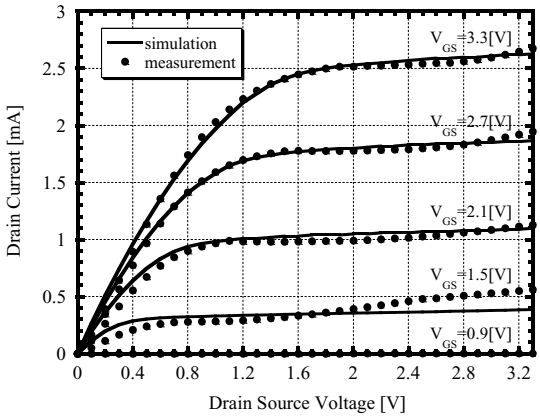
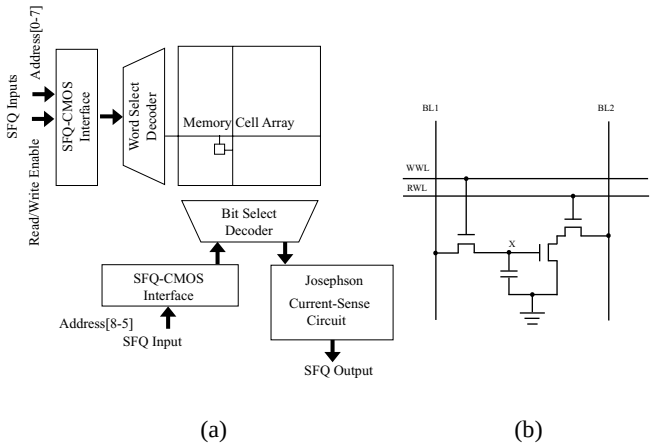


Fig. 1 I-V characteristics of a Rhom 0.35 μm nMOS FET at 4.2 K. Gate width is 4.45 μm. Closed circles are the measured data and the lines are calculated from the BSIM3 device model.



(a) (b)

Fig. 2 (a) Architecture and (b) memory cell structure of the Josephson-CMOS hybrid memory.

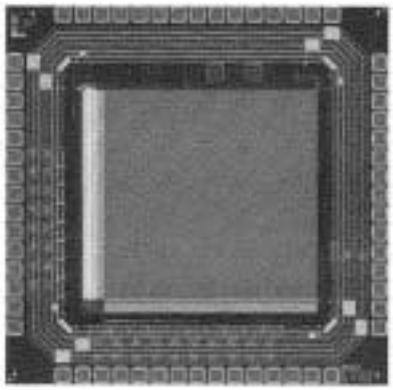


Fig. 3 Photograph of a 16-kbit hybrid memory made in the Rohm 0.35 μm CMOS process. A die size is 2.3 mm.

The Josephson current sense circuit makes it possible to detect the bit-line current at very high speed with low power consumption.

One of the key components in the hybrid memory is a short delay CMOS amplifier, which has to amplify a 40 mV voltage input from Josephson circuits at very high speed. Specially designed differential transconductance amplifiers, whose propagation delay is less than 100 ps, have been designed by using simulation for the 0.18 μm Hitachi CMOS devices. Low-temperature operation of the amplifiers has already been confirmed and a high-speed test is now undertaken.

We have designed a 64 kb SFQ/CMOS hybrid memory and investigated its performance by SPICE simulation using the low-temperature device model. A total access time well below 1 ns is expected from the simulation.

The SFQ/CMOS hybrid memory is fabricated by using the Rhom and Hitachi CMOS process and the NEC Nb standard process [6]. A photograph of a 16 kb CMOS chip fabricated by the Rhom CMOS process is shown in Fig. 3.

A functional test result of a whole memory system except the SFQ-CMOS interface is shown in Fig. 4, where "Address" and "Read/Write" signals with 3.0 V amplitude are applied to the system and "SFQ Output" signals from the system are detected. The figure shows successive operations of "Write 1", "Read 1", "Write 0" and "Read 0". One can see that the transitions in "SFQ Output" appear at the rising edges of "Clock" signals in the "Read1" operation, which corresponds to the output of SFQ signals. A high-speed test is undertaken to estimate the access time. The temperature dependences of the retention time of the memory cell increases exponentially with decrease of the temperature and becomes almost infinite at 4.2 K.

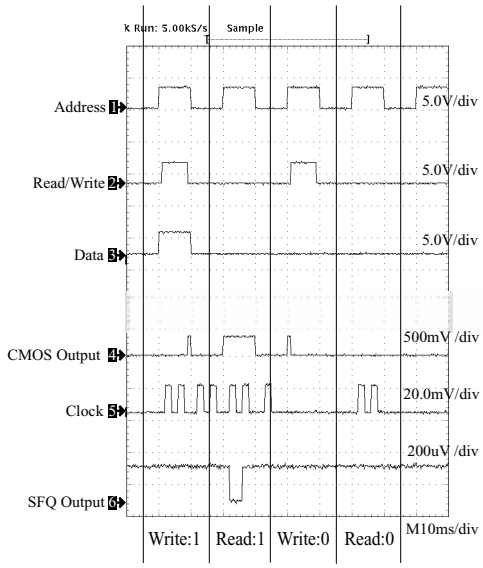


Fig. 4 A low-speed test result of 16 kb hybrid memory system at 4.2 K.

4. Conclusions

Hybridization of SFQ circuits and CMOS circuits may produce a new field of digital systems with very high performance. Recent progress in 4.2 K CMOS device characterization makes it possible to simulate the CMOS circuits with accuracy. It is found from the simulation that sub-nanosecond access time is expected in a 64 kb SFQ/CMOS hybrid memory.

Acknowledgement

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References

[1] K. K. Likharev and V. K. Semenov, IEEE Trans. Appl. Supercond., 1 (1991) 3.
[2] M. Kidono et al., Technical Report of IEICE, SCE2003-39, 2004.
[3] U. Ghoshal et al., IEEE Trans. Appl. Supercond., 3 (1993) 2315.
[4] Y. J. Feng et al., IEEE Trans. Appl. Supercond., 13 (2003) 467.
[5] BSIM3v3.2 MOSFET Model User's Manual, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, 1998.
[6] S. Nagasawa et al, IEEE Trans. Appl. Supercond., 5 (1995) 2447.