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Sub-100nm MOSFET Modeling for Integrated-Circuit Design

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1. Introduction

Device models for Integrated Circuit, IC, design express current and charges as a function of terminal voltages and must be appropriate for implementation in a circuit simulator. Most circuit simulators today implement the direct methods solution of SPICE2/3 developed at UC Berkeley [1]. Sub-100nm MOSFETs exhibit complex behavior and modeling the multitude of physical effects present at these dimensions becomes very challenging.

The requirements placed on such a model are multiple starting with accuracy, computational efficiency, scalability, portability. These requirements are described in Sec. 2.

Several generations of models have succeeded each other keeping pace with technology advancement. Today we witness the overlap of production-proven models such as BSIM3v3 [2] successfully applied to technologies below 0.5µm to 0.13µm, and, the next generation of models like MOS11 [3] and BSIM5 [4], targeted for 90nm and finer technology points. The highlights of these models are contained in Sec. 3.

2. Model Requirements for Accuracy

The SPICE Perspective

Electric simulators such as SPICE use a modified Newton algorithm to solve the nonlinear circuit equations; the nonlinear branch-constitutive equations, BCEs, of transistors are linearized each iteration and a modified node-to-datum admittance matrix is set up. In order for this process to converge the admittances of all nonlinear components must be continuous functions of the terminal voltages [5].

The challenge for modeling MOSFETs has always been the fact that current conduction occurs through diffusion below the threshold and drift above the threshold; therefore the current is expressed by two different current-voltage functions depending on operating region as seen in Fig. 1.

The IC Design Accuracy Perspective

A device model using multiple I-V expressions can introduce discontinuities in the first and higher derivatives. While discontinuities in the first derivative are always a hazard for convergence they may not affect the accuracy of the results for digital circuits which operate mostly between two extremes, *on* (strong inversion), and, *off* (sub-V_T).

Analog circuits on the other hand, can be biased anywhere in the range from positive to negative supply. Modern MOS analog circuits are biased mostly in moderate inversion, the transition region between subthreshold to strong inversion, for maximum gain and reduced power. Additionally, analog circuits are biased in saturation close to the limit with the linear region in order to maximize the output signal excursion. The impact of discontinuities in the first derivatives of the I-V equations can be seen in Fig. 2, where the transconductance of a MOSFET is shown at the transition from weak- to strong inversion. Similar behavior is displayed by the output resistance as a function of V_{DS}.

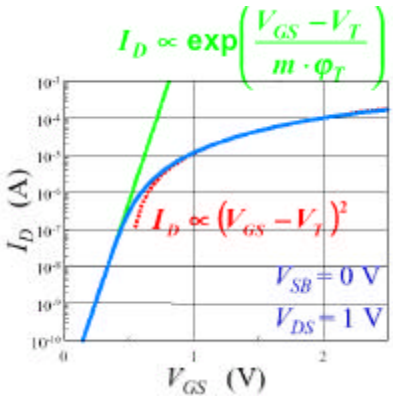

Fig. 1 I_D=f(V_{GS}) for sub- and above threshold

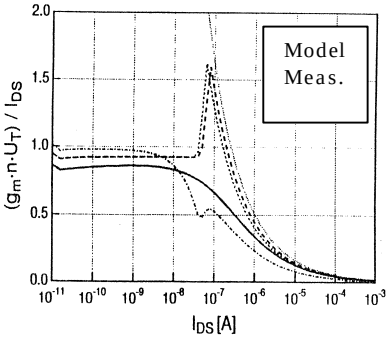

Fig. 2 g_m/I_{DS}=f(I_{DS}) discontinuity in transition region

3. State-of-the-Art MOSFET Models

Device model components

The equations describing the physical behavior of a device need to match actual devices with individual layout geometries, fabricated with specific processes and operating under given external conditions such as bias and temperature. Therefore, model parameters can be classified according to theses three criteria. While roughly half of the transistors in a standard CMOS process share the same process parameters their behavior is a strong function of geometry and operating conditions. The ability of a model through the choice of parameters to match the characteristics of devices fabricated with the same process but with

different geometries is known as *scalability*.

Due to the wide variety of geometry form factors it is impossible to apply the same model parameters to all the transistors sharing the same process parameters. In practice regions of validity of model parameters in the width (W) - length (L) space are defined through a process known as *binning*. Simulators automatically select from a library file containing all *bins* the proper model parameters applicable to a particular MOSFET depending on its dimensions.

Parameter tolerances are becoming increasingly important for the 90nm and 65nm technology nodes where distributions get wider. Today's models and simulators need to provide support for statistics. Extraction programs such as ICCAP or BsimPro are needed to compute with precision the model parameters from measured data.

Current Models

A number of public-domain models, BSIM3, MOS9 and EKV2.6, available in all circuit simulators have been used in recent years. These are semi-empirical models based on device physics, which have done an accurate job of matching current and conductance characteristics of modern complex CMOS structures. BSIM3v3 has been and continues to be the main model for foundries to characterize their processes since the mid-90s and the 0.5µm technology node. The important physical effects are modeled such as short-size effects, reverse short-channel and narrow-width effects, drain-induced barrier lowering, transversal and longitudinal doping-profile impact on threshold, substrate-current induced body effect, velocity overshoot and non-quasi-static effects.

These models are based on the charge-sheet formulation and use the two distinct formulations for subthreshold and strong inversion. They eliminate all discontinuities in the first derivative of the current by using smoothening functions. For scalability with geometry and operating conditions BSIM3 contains parameters and implements dependencies of key process parameters with these variables.

A number of physical effects becoming important in 90nm devices such as gate input current, gate-induced drain current, effective T_{ox} due to quantum-mechanical effects and new dielectric materials, series gate resistance, substrate parasitic network and drain- and source-resistance dependence on V_{DS} led to the introduction of BSIM4.

Next-Generation Models

A new generation of models has been proposed recently which distances itself from the multi-region charge-sheet paradigm. MOS11 has been the first one to formulate the charges and currents based on the surface potential ϕ_S rather than on terminal voltages. Several other models based on surface potential, BSIM5, EKV3, HiSIM and SP, have been presented at the latest Compact Model Council.

All these models start from physical fundamentals and avoid potential pitfalls from smoothening functions, in addition to describing all the relevant physical effects for 90nm and 65nm devices. One challenge of this approach is the need for internal iterations to resolve the nonlinear dependency of ϕ_S on terminal voltages. The models vary on the approximation chosen; based on the observation that ϕ_S varies almost linearly with V_{GS} resolving ϕ_S is fairly efficient and does not require more than three iterations. This formulation also insures the continuity of all charges and their partial derivatives with terminal voltages used to build the circuit admittance matrix.

One other common property of these models is symmetry with respect to drain and source and charge symmetry and reciprocity around V_{DS} =0.

Additional improvements have been brought to the description of noise, distortion and RF behavior. MOS11 implements a very accurate experimentally validated channel and gate-induced noise model. The continuity of the model formulation is proven by the comparison with measurement of second- and third-order predicted distortion terms, as shown for MOS11 in Fig. 3.

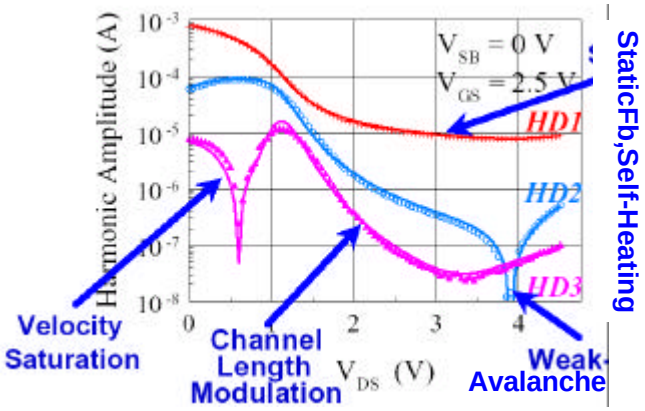

Fig. 3 High-order distortion terms (derivatives) of I_{DS}

The BSIM5 starts from a new core in which it includes many of the BSIM4 formulations. The ϕ_S–based core corrects the non-symmetry problems in BSIM3/4 due to smoothening.

The completeness of these models also comes at the expense of a large number of parameters the reduction of which has become a goal in future developments.

EKV has been the first symmetric-by-construction model referencing terminal voltages to bulk rather than source. It also has a simplified formulation suited for hand calculation and circuit design performance estimation, which have made it a favorite for analog design. EKV3 is also ϕ_S-based

4. Conclusions

A new generation of MOSFET models for sub-100nm devices is being introduced. These models tend to satisfy both the accuracy aspect of behavior and the convergence and computational efficiency of simulation. The near future will impose the next standard for the coming technologies.

References

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