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Low-Voltage-Signaling CMOS Receiver with Dynamic Threshold Control

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1. Introduction

A decrease in supply voltage can markedly reduce the power consumption of LSIs. However, the voltage reduction causes speed performance degradation and a decrease in the noise margin. Conventional LVDS technology [1] has solved these problems by decreasing the signal amplitude and differential signal. For a signal line with large capacity (for example, clock line, data bus, and long wiring between circuitry blocks), such a circuit technique with reduced signal amplitude does not cause performance degradation. However, some problems remain despite these technologies. They are the complex circuitry and increase in power consumption caused by the bias current. By using a low swing signal, a conventional CMOS inverter circuit can have a small circuit area but this results in a small noise margin and an increase in the direct-path short-circuit current. In order to solve these problems, we propose a dynamic threshold control CMOS receiver (DTCR). The proposed DTCR makes it possible to enhance the noise margin for high-frequency noise and decrease the power by controlling the logic threshold voltage dynamically. In this paper, we report on the operating characteristics of the DTCR test circuit consisting of a variable-channel-size MOSFET (VS-MOS) [2].

2. Dynamic Threshold Control CMOS Receiver

Figure 1 shows the schematic of the DTCR. The DTCR consists of a signal delay part, a variable logic threshold inverter (VT-INV) [3]. The VT-INV consists of two VS-MOSs. Figure 2 shows the layout of a VS-MOS and Figure 3 shows the circuit of the VT-INV. The VS-MOS is a MOSFET which can modulate the effective channel size continuously with the control gate voltage [2]. The VT-INV can modulate the logic threshold using the terminal voltage Vcnt [3]. Figure 4 shows the logic threshold of a VT-INV test circuit (gate width of p-ch, Wp=21µm, and n-ch width, Wn=7µm; gate length L=Lc=0.35µm, WS=6.0µm, Sv=0.375µm) when the Vcnt was changed from 0.0V to 3.0V; the logic threshold voltage smoothly changed from 1.8V to 0.7V. The logic threshold voltage of the VT-INV can be modulated by up to 1.1V continuously. The time chart of the DTCR's signals is shown in Figure 5. The DTCR creates a large noise margin by inputting the delayed signal into the control terminal of the VT-INV. If the input signal cycle is longer than the delay time "Td", the DTCR detects the input signal as "signal". If the input signal cycle is shorter than Td, the DTCR regards the input signal as "noise" and no response is observed. The test circuit uses two inverters for the delay part, and Td can be controlled by changing the delay part parameters.

3. Fabrication of Test Circuit

A test circuit is fabricated using a normal 0.35µm CMOS by the 1-Poly, 3-Metal process. The VT-INV of this test device has the following characteristics: Wp=24µm, Wn=7µm, L=Lc=0.35µm, Sv=0.375µm, WSp=4.0µm, and WSn=6.0µm. Those of the buffer CMOS inverter are Wp=21µm Wn=7µm, and L=0.35µm, and those of the delay part inverters are Wp=6µm Wn=2µm, and L=0.35µm. Figure 6 shows a photomicrograph of the DTCR test circuitry. The circuit area is 40µm×13µm.

4. Measurement Results

Figure 7 shows the measured waveforms of the DTCR's signals. The input signal is a mixed signal composed of a 400mV amplitude (1.20～1.60V) base signal and a 2.3V amplitude sine wave of 257MHz. Figure 7 shows the measured noise filtering characteristics of the DTCR. It shows a stable output against the noise that has an amplitude larger than that of the input base signal. Figure 8 shows the measurement result of the noise filtering characteristics. This circuit has a redundant capacitance of 4pF for both measuring and monitoring circuits. The gray line shows an estimation of the noise filtering characteristics of the DTCR with the redundant capacitance removed. The DTCR can remove the noise more sharply than conventional CMOS inverters (such as a low pass filter). The proposed DTCR has a sharper filtering property for high frequency noise. Figure 9 shows estimation of power consumption of DTCR as a function of signal amplitude in the case of the input capacitance of 3pF and signal frequency 200MHz. In the case of signal amplitude 400mV, the power consumption of the DTCR is a one-sixth that of the conventional CMOS circuit.

5. Conclusion

A CMOS receiver employing dynamic threshold control is proposed. The proposed DTCR can be realized with a simple CMOS circuit using VT-INV consisting of two VS-MOSs. The characteristics of the DTCR are evaluated using a test circuit, and the property of high-frequency-noise filtering is confirmed.

Acknowledgment

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References

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[3] Y.Kosasayama, Y.Arima, M.Ueno, M.Kimata, K.Himei, and T.Asano, IEICE VOL.E87-A No.2 Feb 2004 pp.357-363

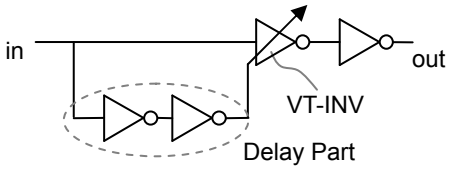

Fig. 1 Dynamic Threshold Control Receiver (DTCR).

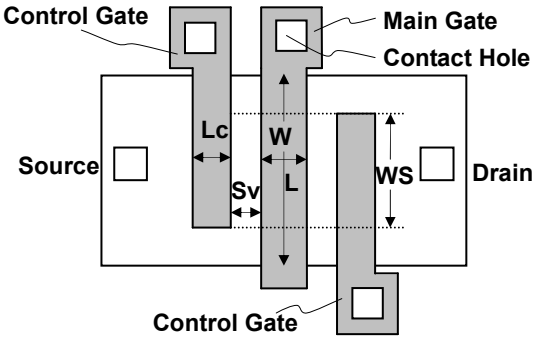

Fig. 2 Layout of VS-MOS.

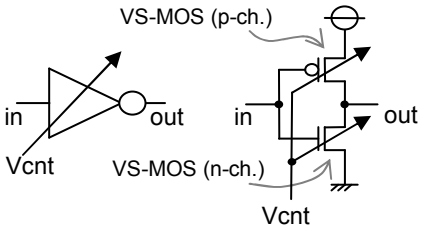

Fig. 3 Variable Logic Threshold Inverter (VT-INV).

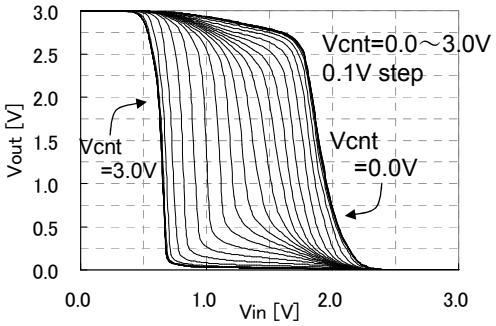

Fig. 4 Measured transfer curve of VT-INV (Wn/Wp=7μm/21μm, L=0.35μm, Lc=0.35μm WS=6μm, Sv=0.375μm).

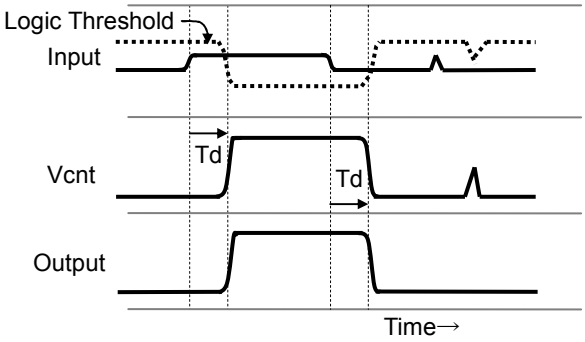

Fig. 5 Time chart of DTCR.

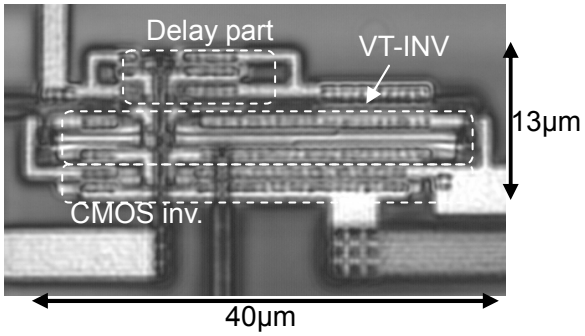

Fig. 6 Photomicrograph of DTCR test circuit.

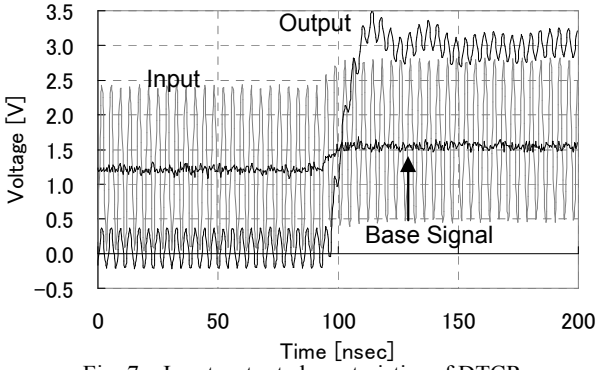

Fig. 7 Input-output characteristics of DTCR.

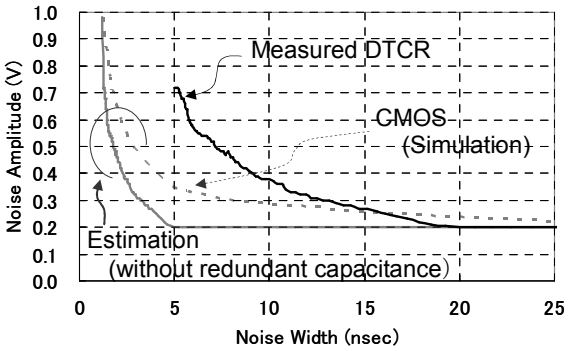

Fig. 8 Measurement result and estimation of noise filtering characteristics of DTCR.

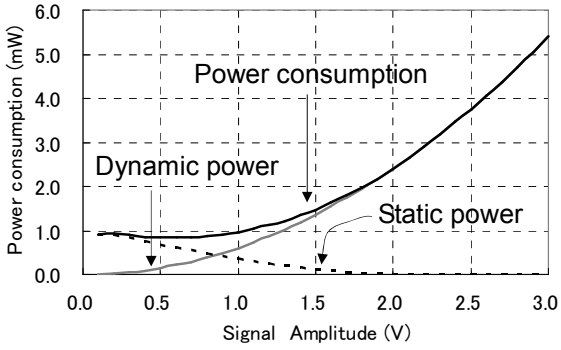

Fig. 9 Estimation of power consumption of DTCR as a function of signal amplitude in the case of the input capacitance of 3pF and signal frequency 200MHz.