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A CMOS Monocycle Pulse Generation Circuit of UWB Transmitter for Intra/Inter Chip Wireless Interconnection

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1. Introduction

Steady downscaling of semiconductor device dimensions has led to the concept for wireless interconnection (shown in Fig. 1) within the chip and among the chips to avoid transmission delay due to parasitic effects of conventional wiring [1]. For high data transmission rate and multiple access capability of the wireless interconnection system, it requires wideband characteristics of integrated transmitter and receiver. A Time Hopping-Ultra Wideband (TH-UWB) transmitter (shown in Fig.2) generally transmits very short duration Gaussian monocycle pulses without a sinusoidal carrier [2]. Such monocycle pulses can be generated from time hopped signal (THS) by using a step recovery diode (SRD) based circuits with pulse shaping and differentiation network [3]. But, the variation in pulse position due to temperature, the low pulse repetition rate and fabrication of SRD on the same substrate limits the use of SRD based circuits for such an application. Thus here, we report a new technique based on current CMOS technology to generate monocycle pulses for a single chip TH-UWB transmitter.

2. Monocycle Pulse Generation Circuit

The developed monocycle pulse generation circuit consists of RLC network along with RC filter, pulse generation (PG) circuit and transmission gate as shown in Fig. 3. The RLC network with RC filter produces a damped sinusoidal signal from a Short Rectangular Pulse (SRP) train which is generated from Time Hopped Signal (THS) using PG. The frequency of oscillation (f) of damped sinusoidal signal is found as

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R}{4L^2}} \qquad (1)$$

Where R = resistance, L=inductance and C =capacitance of the RLC network. This damped sinusoidal signal (Vosc) is then passed through a transmission gate which is controlled by a pulse with a width of (1/f) to pass the first cycle of the signal at the output (monocycle). The transmission Gate Control Pulse (GCP) is also generated from the same THS by using PG. The PG circuit consists of a voltage controlled delay, Exclusive-or (EXOR), NAND, Inverter and non-inverting buffer circuits as shown in Fig. 4. The voltage controlled delay consists of a cascaded inverter pair with an additional series-connected NMOS transistor in the pull down of each inverter controlled by a global control voltage (V_{n1}) and its delay is inversely proportional to the square of the control voltage. The voltage controlled delay circuit produces time shifted THS which is then applied along with THS as inputs of EXOR. The output of EXOR and THS are then passed through NAND and inverter to produce SRP and GCP for the RLC network and transmission gate respectively.

3. HSPICE Simulation results

The circuit simulation is done from the extracted layout netlist by HSPICE for TSMC 0.18 μm CMOS process. The simulated output response of the delay circuit of PG for different transistor sizes is shown in Fig. 5. The simulation shows that a short pulse of minimum width of 0.1ns could be generated using the PG. The PG generated SRP and GCP from a THS of width 1.25ns is shown in Fig. 6. The figure shows that rising edge of the SRP and GCP occurs at the same time. The gate control pulse with width of 0.4 ns is generated here because the RLC network along with RC filter generates a damped sinusoidal signal with frequency of 2.5 GHz as shown in Fig. 7. This frequency limitation is due to the use of available low inductance in TSMC library. This frequency can be increased by using low value of inductance and capacitance and short GCP. The transmission gate output is shown in Fig. 8. The figure shows the generated monocycle pulse (MCP) is symmetry with a peak to peak amplitude of 0.5v. This symmetry is obtained by proper sizing of the transmission gate transistors. A FFT of the monocycle pulse is shown in Fig. 9 which shows that the generated monocycle pulse has a wide bandwidth of about 2.9 GHz. A performance data is shown in Table 1 and chip layout is shown in Fig. 10.

4. Conclusion

The proposed monocycle pulse generator is implemented using the current CMOS technology. The developed monocycle pulse consumes low power (4.4mw) and occupies a small area (0.19mm^2). This will lead to develop a single chip UWB transmitter for intra/inter wireless interconnection.

Acknowledgements

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References

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[2] Moe Z Win and R. A. Scholtz, IEEE Trans. on communications, vol. 48, No. 4, April 2000, pp. 679-691.
[3] Jeongwoo Han and Cam Nguyen, IEEE microwave, wireless and components Letters, vol. 12, No. 6, June 2002, pp. 206-208.

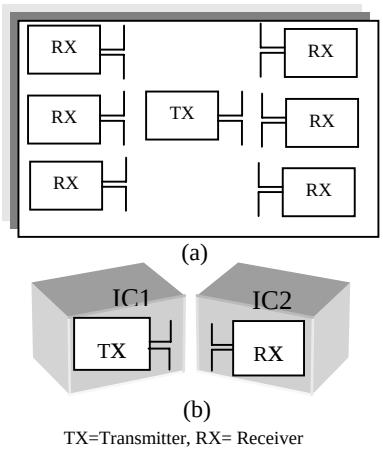

Fig.1 Wireless interconnection : (a) Intrachip (b) Interchip.

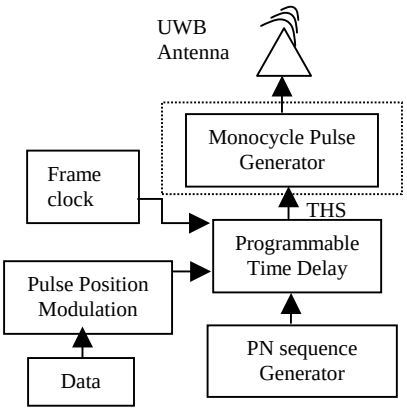

Fig.2 Schematic of a TH-UWB Transmitter.

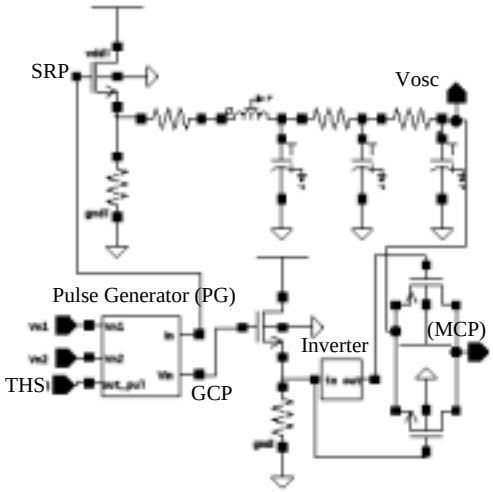

Fig.3 Monocycle pulse generator circuit.

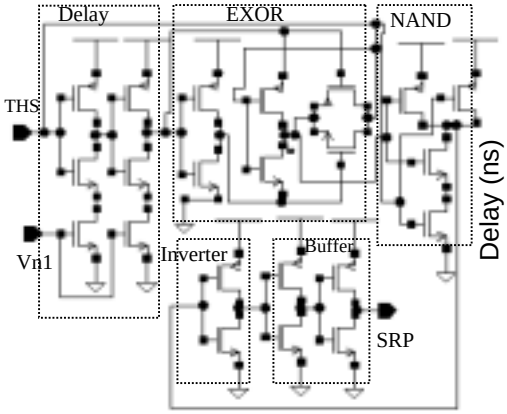

Fig. 4 A Pulse Generator (PG) circuit to produce SRP for RLC network. An identical circuit is used for generation of GCP (not shown here).

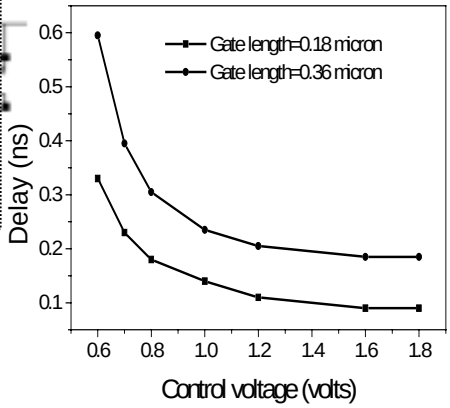

Fig. 5 Variation of delay with Control voltage.

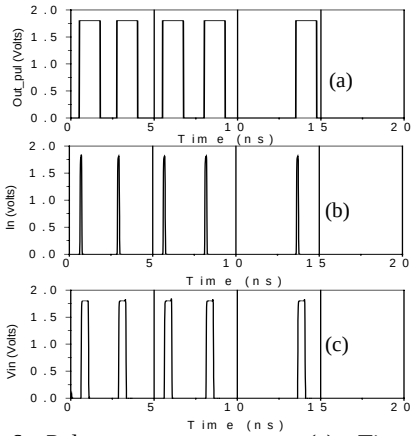

Fig. 6 Pulse generator response (a) Time hopped signal (THS); (b) short rectangular pulse (SRP) and (c) Gate Control pulse (GCP).

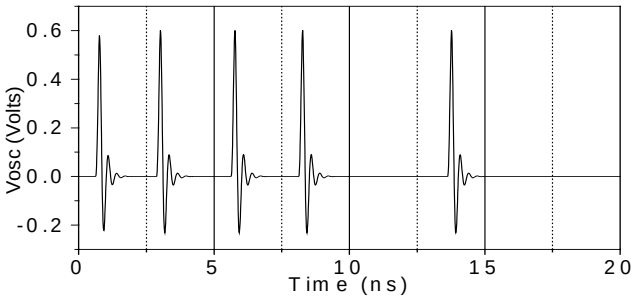

Fig. 7 Damped sinusoidal wave (Vosc).

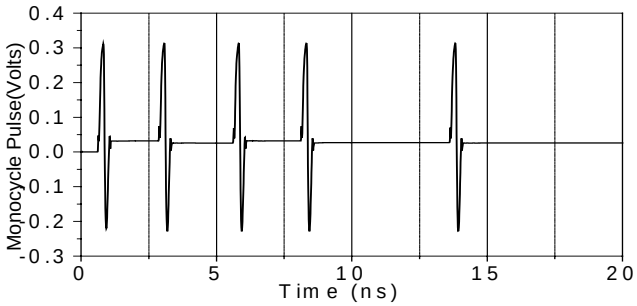

Fig. 8 Time-hopped monocycle pulse (MCP) train.

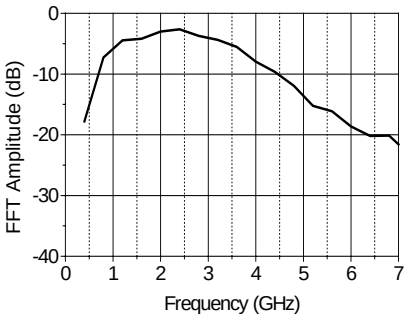

Fig. 9 FFT of monocycle pulse.

Table I Performance Data

Monocycle peak to peak amplitude	0.5 v
Power consumption	4.4 mW @ 1.8v
Monocycle center frequency	2.5 GHz
3 dB Bandwidth	2.9 GHz
Chip Area	0.19 mm^2
Technology	TSMC 0.18 µm CMOS mixed signal process

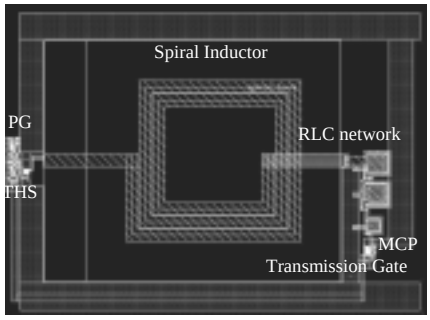

Fig. 10 Chip layout.