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A Right-Brain/Left-Brain Integrated Associative Processor Employing Convertible MIMD Elements

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1. Introduction

Despite the enormous computational powers of digital processors, human-like flexible information processing is not possible yet. In order to solve the problem, a psychologically-inspired VLSI (right-brain computing VLSI) system has been proposed [1], where the associative processor plays an essential role. The associative processor is a dedicated search engine chip that finds out the most similar vector to an input vector from the vast collection of template vectors representing the past experience of a human [2,3]. Using the chip, robust image recognition has been demonstrated [4]. Since the flexible recognition is carried out not by logical deduction but by intuition through the association to the past experience, the processing is called right-brain computing. In order to carry out human-like flexible recognition, however, the associative processing (right-brain computing) only is not sufficient and certain logical deduction processing is inevitable. When we recognize something, we first capture primitive information such as patterns and motions of the target object and then, we recognize the target by logical thinking of the primitive perception results. Such a high-level logical processing or if-then-else-like processing, we call left-brain computing in the analogy to the partition of functions in the right and left hemispheres of our brains.

The purpose of this work is to propose a new-architecture MIMD (Multiple Instruction-stream Multiple Data-stream) associative processor VLSI in which each MIMD element can work as a regular CPU while keeping the high performance as an associative processor. For this purpose, three key technologies have been developed: right-brain/left-brain-function convertible MIMD element for efficient computation; versatile register control scheme within the MIMD element; short-length instruction set for minimizing the memory size for program storage. The last issue is important because the memory resources must be preserved for as many as possible template vectors to use in associative processing. Almost all core circuit blocks were implemented using Verilog and the test circuit of the MIMD element was layouted and fabricated.

2. Right-Brain/Left-Brain-Function Convertible MIMD Element

The MIMD associative processor architecture developed in this work is shown in Fig. 1. It is composed of eight MIMD elements, each working independently according to the instruction-stream given to the element. Each MIMD element is composed as a SIMD (Single Instruction-stream Multiple Data-stream) processor having eight parallel SIMD elements. The function of a MIMD element is convertible to either an associative processing (right-brain computing) or a regular CPU processing (left-brain computing). The convertibility of the architecture is realized by introducing a special ALU. The architecture of the ALU is firstly explained in the following.

The ALU in each SIMD element consists of three processing blocks: “Add/Bit”; “Sign/Booth”; “Shift/Accumulate”, as shown in Fig.2. The ALU has two modes, the associative mode and the arithmetic mode. In the associative mode, it calculates the Manhattan distance between the input vector and a template vector by connecting the three blocks in series. In the arithmetic mode which is used to realize the logical processing, the ALU selects some of the processing blocks and executes one arithmetic operation selected from adding operation (add, subtract), bit operation (and, or, xor), shifting operation and multiplying operation.

The various arithmetic operations have been realized by adding small circuitries to the conventional associative processor [2]. The Booth decoder introduced to the present system allows efficient multiplication by converting 8-bit multiplication to 4-cycle shift and add operations.

If all the MIMD elements work for the associative processing, all the 64 SIMD elements calculate distances in parallel, thus making the system a high-performance associative processor.

3. Register Architecture in MIMD Element

To realize the regular CPU processing such as decision or repetition, the SIMD controller in each MIMD element plays an essential role. It contains an instruction decoder and control registers such as a status register or an instruction cache register. All registers are 64bit (8 parallel 8bit) width.

Fig. 3 illustrates how “loop” and “subroutine call” are realized. The stack register reduces memory access storing up to four 16bit status data for 8bit instruction address, 4bit program counter of the instruction cache register and 4bit loop counter. The loop and subroutine functions are realized by managing the status values.

One of the notable features of the present architecture is the introduction of parallel/serial (P/S) registers in data registers. A P/S register has an 8bit x 8 words (64bit) con-

figuration and has two access modes: parallel access and serial access. In the parallel access, 8 words are simultaneously accessed and write/read operations are carried out in parallel. In the serial access, only one-word register in the P/S register is accessed. In the write cycle, one word of data is written. But in the read-out cycle, one word of data selected from 8 words of data in the P/S register is copied and the identical data are broadcasted to the output. This mode of operation realizes efficient vector processing such as internal product or transposing.

A MIMD element including above mentioned features was designed in a 5-metal 0.18µm CMOS technology as shown in Fig. 5. It has been confirmed on logical simulation. "Add/Bit" calculators are employed as ALU instead of the convertible ALUs because the evaluation of the versatile register control architecture is of primary concern. The ALU functions were designed as a separate test chip. The MIMD element occupies 1mm x 2.5mm area. Therefore a full integration of the chip shown in Fig. 1 with enough amount of memory is feasible with a chip size of $1cm^2$.

4. Short-Length Instruction Set

The short-length instruction set has been developed to realize various instructions in a small size of instruction data. This instruction set has instruction groups which are switchable as a result of preserving the group bit in the instruction decoder and using the instruction-group switching instruction. To reduce the group-switching overhead, the alias instruction is prepared. The alias instruction can assign an instruction of another group to a prepared empty instruction of each group. Using the method mentioned above, over seventy 8bit-instructions in eight groups (3bit) are constructed for the MIMD associative processor.

5. Conclusions

A new-architecture MIMD associative processor is proposed featuring right-brain/left-brain convertible functions. The architecture was designed with a full set of instructions. Almost all core circuits were implemented with Verilog and the MIMD element was layouted. As a result, the feasibility of 8 parallel MIMD chip has been confirmed.

Acknowledgements

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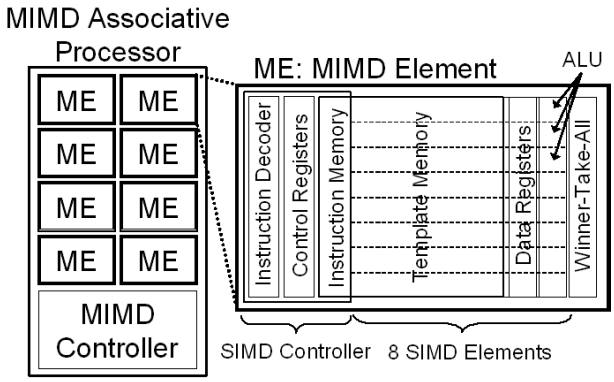

Fig. 1. Organization of MIMD Associative Processor.

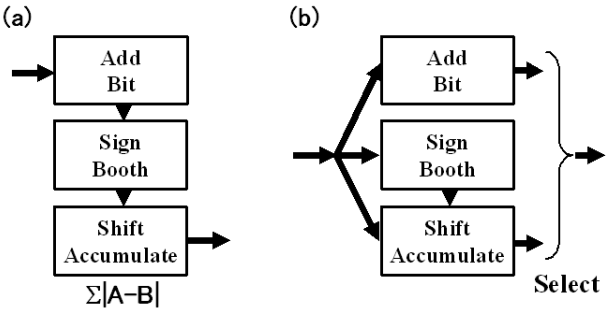

Fig. 2. Two modes of ALU: (a) associative mode and (b) arithmetic mode.

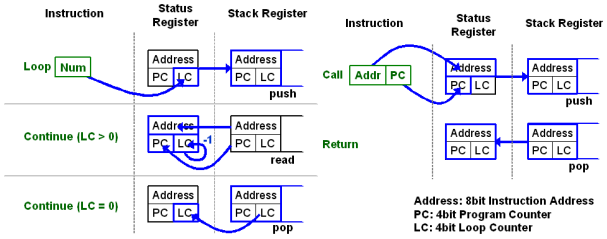

Fig. 3. "Loop" and "subroutine call" using stack register.

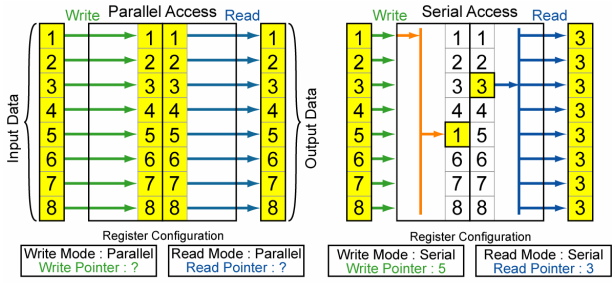

Fig. 4. Two access modes in parallel/serial register.

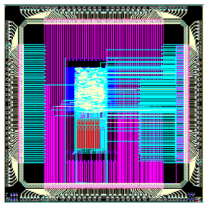

Fig. 5. Layout of prototype MIMD element.