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# Design of RFID Front-end Circuitry Enabling CDMA-based Collision Resistance

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## 1. Introduction

Rapid market growth of RFID systems necessitates a large capacity of collision resistance in simultaneous tag recognition[1]. We have proposed a communication scheme for an RFID system that can recognize multiple tags up to a thousand in 300 msec, featuring anti-collision, error correction, and re-transmission[2].

In this paper, we propose a design of RFID front-end circuitry including a synchronization circuit, a modulator, and a demodulator for enabling CDMA-based collision resistance.

## 2. Circuit Architecture

An RFID system consists of transponders and a reader. Tags incorporating a transponder are installed on each item to be identified, and they begin to respond when entering the interrogation zone of a reader. A reader identifies each ID number responded by transponders. For a battery-less operation of transponders, power is supplied through inductive coupling from a reader.

Proposed sequence of identification between a reader and a transponder is shown in Fig.1. During receiving power-wave from a reader, a transponder is active and waiting 180-degree phase shift (thus invert) of the power-wave for synchronization. After completing the synchronization, the transponder selects a channel and starts to transmit ID on the basis of CDMA modulation. Then the reader correlates the received signal to demultiplex IDs. In the sequence, synchronization and passband modulation play an important role, which are detailed in later sections.

Proposed RF circuits for a transponder and a reader are depicted in Fig.2 and Fig.3, respectively. The transponder RF front-end circuit includes a rectifier, a modulator, a timing generator, a voltage limiter, and capacitors. The reader has an RF front-end circuit followed by Analog to Digital Converter(ADC) and Digital Matched Filter(DMF) for correlation. The reader RF front-end eliminates the carrier of 13.56 MHz and then amplifies the extracted modulation signal with 6.78 MHz band width. The signal is demodulated by ADC, and then despread by DMF.

### Synchronization Control

Synchronization between transponders and a reader is important in CDMA, because the spread information received must be correlated to local spread codes within an identical time-frame. A reader shifts the phase of the transmitting wave to 180-degree in a cycle to notify a synchronize criterion to transponders. Hence, both a reader and transponders work in a synchronized time-frame.

The synchronization circuit of a transponder is realized by using an SRFF and a DFF as shown in Fig.2. When the wave is inverted, the "set" input of the SRFF rises up twice successively, and its state holds high in two cycles. As the clock of the DFF is equivalent to the "set" input, the state of the DFF is toggled to high at second raise and holds high in a cycle, as shown in Fig.4. Consequently, the inverted wave is detectable in this simple way.

### Passband Modulation

We propose a modulation method that can reduce power consumption and circuit area of transponders. In the transponder RF circuit, the charge accumulated in the capacitor $C_P$, which is rectified from power-wave transmitted by a reader, passes the current to the antenna coil by a PNP transistor, and it induces a counter electro-motive force in a reader antenna. As shown in Fig.5, two impulses, which are depicted in shadow, modulate signals. They appear when the falling sinusoid transmitted by a reader crosses to zero, and they express "0" by two successive negative pulses, while "1" by positive. Thus, they have a frequency component of 6.78 MHz, which is half to the carrier of 13.56 MHz. Finally the RF circuit can extract the signal component through carrier elimination followed by low-pass amplification.

## 3. Simulation Results

### Transponder Operation

We had designed the circuit of Fig.2 in a 0.18 $\mu$m digital CMOS technology and simulated the operation with HSPICE circuit simulator. The waveforms are shown in Fig.6. The modulation timing is given by a zero cross detector, and the synchronization timing of CDMA is given by a synchronization circuit of a transponder. The transmitted power is accumulated to capacitors through a rectifier. The simulated waveform shows these modules work correctly. Hence, it is validated that a timing generation circuit correctly detects zero cross positions and generates inverted pulses to the logic part.

### Reader Operation

We also simulated demodulation circuit by MATLAB mathematical simulator by building an abstract model of ideal inductive coupling between a transponder and a reader. The reader RF circuit is behaviorally modeled as a low-pass filter whose AC response is shown in Fig.7. The amplitude ratio of modulation impulse to the carrier is 1 : 20, which is derived from HSPICE simulation of a transponder. A transponder modulates a logic "1" at first, then "0" after 20 cycles as shown in Fig.8. Then, the output of the reader RF circuit has two large peaks showing received data, along with decaying vibrations. This proves that ID information can be successfully transmitted from a transponder to a reader through the proposed modulation/demodulation scheme.

## 4. Conclusion

This paper presented design of RF circuitry of a transponder and a reader for a highly collision resistive RFID system. Simulation demonstrated the proper operation of a synchronization unit and a modulation circuit. Fabricated IC chips based on the proposed architecture is under testing.

## References

[1] K. Finkenzeller, *RFID-Handbuch*, Carl Hanser Verlag, 1998.
[2] Y. Fukumizu et al., "A Highly Collision Resistive RFID System", *in Proc. of APSITT 2003*, pp. 223–228, 2003.

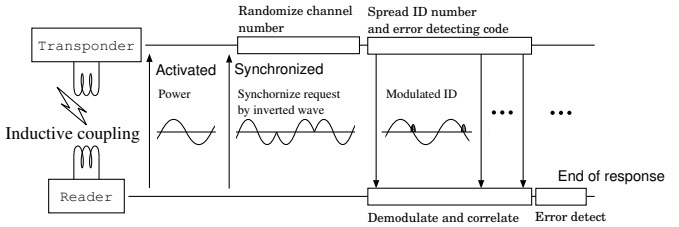


Fig. 1: Communication sequence of RFID system

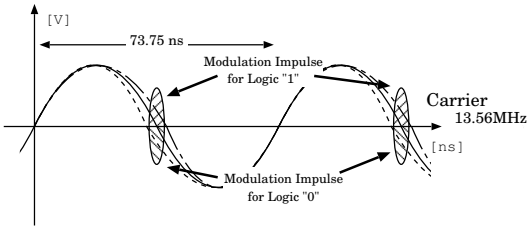


Fig. 5: Modulation waveform

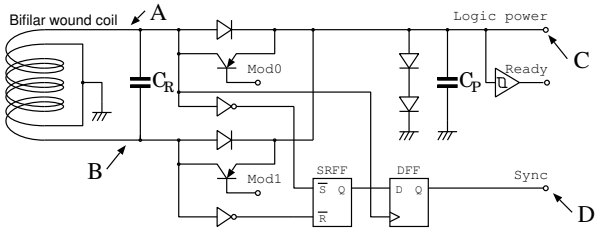


Fig. 2: Transponder RF circuit diagram

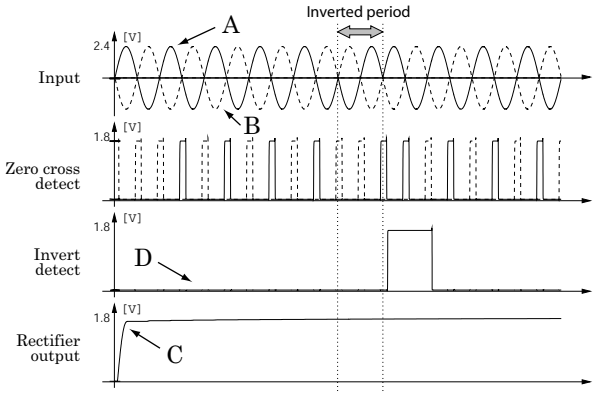


Fig. 6: Simulated time-domain waveform

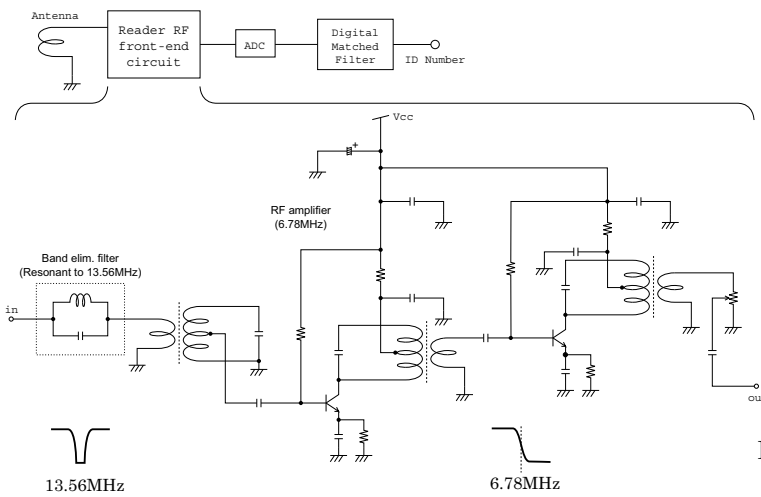


Fig. 3: Reader RF circuit diagram

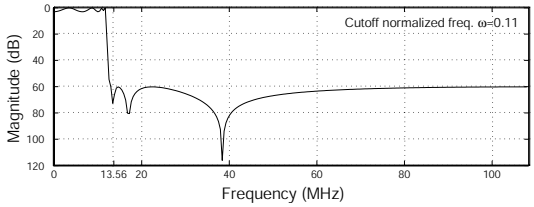


Fig. 7: Simulated AC response of reader RF circuit

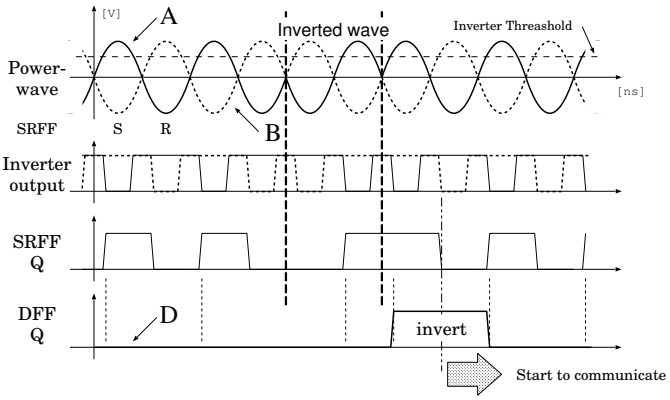


Fig. 4: Synchronization timechart

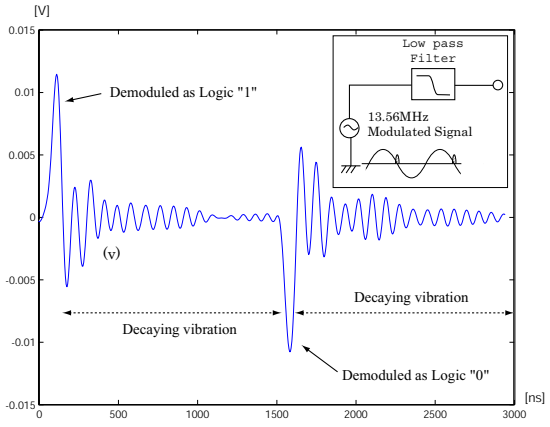


Fig. 8: Simulation of demodulation