Indium selenide based phase change memory

Heon Lee¹ and Dae-hwan Kang²

¹Korea University, School of Engineering, Department of Materials Science and Engineering Anam-dong 5Ga-1, Sungbuk-Gu, Seoul 136-701, Korea Phone: +82-2-3290-3284 E-mail: heonlee@korea.ac.kr
²Korea Institute of Science and Technology, Thin Film Materials Research Center Hawolgok-dong 39-1, Sungbuk-Gu, Seoul 136-791, Korea

1. Introduction

As many newly developed digital electronic devices such as digital camera and camcorder, MP3 player, smart phone and so forth become popular, the demand for non-volatile memory is significantly increasing. Since NAND or NOR type Flash memory is only available non-volatile memory, its market size begins to exceed that of DRAM (dynamic random access memory).

Various kinds of non-volatile memory devices have been studied. The two most typical new non-volatile memories are FRAM (ferroelectric random access memory) and MRAM (magnetic random access memory). FRAM has been studied more than a decade by many researcher groups. Although commercial production of FRAM is achieved, its production volume is almost negligible. Many fundamental problems including fatigue of ferroelectric materials and process integration issue needs to be solved. As an alternative of FRAM, MRAM, which utilize TMR (tunneling magneto-resistance) junction, gains huge interest due to its very fast switching speed and infinite reading cycles. However, fabrication of large MRAM array with narrow distribution of electric characteristics proved to be extremely difficult. 'Half select" is another obstacle of MRAM to be overcome. Since such problems become severer with shrink of device size, future of MRAM as a standalone high density memory is not very clear.

Phase change memory, so called PRAM is a new non-volatile memory which uses reversible phase transition of chalcogenide resistor. Compared to FRAM and MRAM, PRAM has several advantages including (1) extremely large read dynamic range, (2) reduced switching current and improved device reliability with reduced device size and (3) potential multi-bit per cell operation. Therefore very extensive research work is on going in order to commercialize PRAM as a standalone memory and a memory unit for SOC (system on a chip). [1], [2]

The basic switching mechanism of PRAM is as follows. The phase of chalcogenide resistor was controlled by electric pulse. By high and short pulse, chalcogenide resistor was rapidly heated up to its melting temperature and the quenched. Thus phase of chalcogenide becomes amorphous phase. By low and relatively long pulse, chalcogenide resistor was heated below to its melting temperature. Just like an annealing effect, amorphous phase chalcogenide becomes crystalline phase. Since the electric resistivity of amorphous chalcogenide is orders of magnitude higher than that of crystalline chalcogenide, phase transition of chalcogenide can be easily sensed.

2. Experiment

Indium selenide phase change material

Typically $Ge_2Sb_2Te_5$ compound, which is developed for optical data storage such as CD-RW and DVD-RW, is widely used as a phase change resistor material. When as sputtered, amorphous $Ge_2Sb_2Te_5$ compound is crystallized by isothermal annealing, its electrical resistivity changed up to 10^3 times.

In this study, In based chalcogenide (In_2Se_3) was chosen due to its wider change of electric resistivity (up to 10^5 times) and higher resistivity than Ge₂Sb₂Te₅ compound. TEM photographs of as grown and annealed In₂Se₃ thin film are shown in Figure 1. According to 4 point probe measurement, relative electric resistivity of amorphous In₂Se₃ film is 3 x 10^4 times higher than crystalline film.



Fig. 1. TEM photograph of as grown amorphous In_2Se_3 film and annealed crystalline In_2Se_3 film.

Cross point device fabrication for test

Cross point type test PRAM devices are fabricated with In_2Se_3 resistor. On the oxidized Si wafer, Mo film was patterned to make bottom electrode then PECVD Si oxide film was grown. Contact holes (via) are patterned with photolithography and etched with RIE. Although the linewidth of bottom and top metal is large, actual PRAM device size is determined by this contact hole fabrication. Then phase change layer (In_2Se_3 film) and top electrode (Mo) layers are

deposited and patterned. Typical cross-sectional and top view of PRAM test structure is shown in Figure 2.



Fig. 2. Typical cross-section and top view of PRAM test device.

3. Results and Discussion

Static mode measurement

Static mode switching of PRAM device is shown in Figure 3. In first sweeping, as grown amorphous In_2Se_3 resistor shows high resistivity. However, when it reached threshold voltage, electrical resistance of device is drastically reduced. Some kind of electrical conducting path is formed by this step. After the first sweep, device resistance decreased.



Fig. 3. Static mode I-V characteristics of In_2Se_3 based PRAM test device.

Pulsed mode measurement

Pulsed mode switching behavior was measured after sweeping the device in static mode. The result of pulsed mode switching of PRAM device is shown in Figure 4. 70ns, 3.1V short pulse was used to reset (crystalline \rightarrow amorphous) the device and 10 µs, 1.2V long pulse was used to set (amorphous \rightarrow crystalline) the device. Reading is done by measurement of device resistance at 0.2V. Switching dynamic range (ratio of R_{high} to R_{low}) was as high as 100. In Figure 5, resistance of In₂Se₃ PRAM device under various set pulse height is shown. By adjusting set pulse height, resistance can be set to any value between 3 x 10³ ~ 1 x 10⁶ ohms. Since the amount of heat input into chalcogenide resistor is determined by applied set pulse height, the degree of crystallization of resistor is also altered by applied set pulse height

3. Conclusions

Cross point type, In_2Se_3 based PRAM device was fabricated and tested. The devices were successfully switched with 4. 70ns, 3.1V pulse for resetting and 10 μ s, 1.2V pulse for

setting.

Acknowledgements

We would like to thank to TND for financial support.

References

[1] Research report from Ovonics, <u>http://www.ovonic.com/PDFs</u> /Elec Memory Research Report/OUM.pdf, (1999).

[2] S. Lai, Tyler Lowrey, International Electronic Device Meeting Technical Digest, (2001).

[3] S. Lai, International Electronic Device Meeting Technical Digest, (2003).



Fig. 4. Pulsed mode switching behavior of In_2Se_3 based PRAM test device. Up to 100 of switching dynamic range is observed.



Figure 5. Resistance of In₂Se₃ PRAM device under various set pulse height.