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Distribution and Impact of Local Trapped Charges in SONOS Memory

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1. Introduction

Different from the floating gate Flash memory, SONOS memory is a kind of charge trap device, which uses a multi-layer Oxide/Nitride/Oxide (ONO) as the gate dielectric and usually programmed by CHE or CHISEL injection [1]. It is quite different from Flash memory for the charges can be stored in a local narrow region, which makes SONOS devices more complex than the floating gate ones. Papers [2][3] have given an approximate model containing a series of two MOSFETs. In this paper, we propose a model considering the punch-through effect and discuss on the impact of the narrow distribution of the trapped charge injected by CHE or CHISEL programming.

2. Cell Structure and Model

The W/L of the fabricated SONOS sample is 20μm/0.8μm, with the thickness of the ONO being 4.5nm/8nm/5nm. During CHE programming, the hot electrons are trapped in the Nitride layer near the Drain side, as shown in Fig.1a, formatting a short channel transistor (M_S) with higher threshold voltage and a long channel transistor (M_L) with native V_{T0}. However, the lateral distribution of the trapped charges is usually rather narrow (less than 80nm [4]) and near the drain junction, which will lead to the punch-through leakage current (I_{PT}) between the inversion channel below M_L and the Drain (in Fig.2, simulated in SILVACO). In order to describe I_{PT}, we introduce a changeable resistor (R_{PT}) connected parallel to the transistor M_S, as shown in Fig.1b.

With this model, the I_d-V_g characteristic in read mode is no longer the same with the conventional floating gate one. Actually, it can be divided into three regions: Sub-threshold region, Transition region and Turn-on region. In the Sub-threshold region, M_S with larger V_T is off and can be neglected, therefore R_{PT} and M_L dominate the performance of the whole cell; In the Transition region, with the rising of V_g, the equivalent resistor of M_S begins to decrease, which reduces the sub-threshold slope of the I_d-V_g curve [4][5]; In the Turn-on region, M_S is already turned on and dominates the cell's performance.

3. Simulation and Experimental Results

Fig.3 shows the typical characteristics of I_d-V_g after different program time, presenting to different density of trapped electrons. Curve B and C have a narrower charge distribution than curve D, resulting in larger I_{PT}.

Also, simulation results are shown and fitted with the experimental data well in the Sub-threshold region. The difference in the Turn-on region is due to the actual Gaussian distribution of the trapped charges, and the V_T is determined by the peak value of the charge density, however, it is set to the rectangle-like distribution in simulation.

This narrow distribution of local-trapped charges will prevent the turn-off voltage (V_{off}, defined as the voltage when $I_d=10^{-9}$A) rising until the saturation of V_T and lead to a leakage current of the unselected cell, as shown in Fig.4.

Program condition optimization, CHISEL program method and cell structure optimization, such as reducing the depth of the drain junction or adopting the punch-stop halo implantation, have been demonstrated to be able to improve the distribution of the trapped charges and decrease the sub-threshold leakage current. Fig.5 illustrates different read curves with different programming gate voltage. A higher V_g forms a stronger vertical electric field, which makes the trapped charge distribution narrower and nearer to the drain junction and leads to smaller shift of I_d and V_{off} in the Sub-threshold region. The optimized gate voltage is a little higher than V_D.

Fig.6 shows the comparison of CHISEL and CHE program. It is clear that ΔV_{off} with CHISEL programming is higher than the one with CHE programming, whereas both of the ΔV_T are almost of the same. The reason lies in that the trapped charge region during CHISEL is much wider than during CHE, and is far from the drain junction, (see Fig.7, the trapped electron distribution along channel, using Charge Pump method) therefore decreasing the punch-through caused leakage current.

Fig.8 is the simulation results with different junction depth. It is clear that the punch-through leakage current can also be obviously reduced with the shallow junction

4. Conclusions

In this paper, a model with R_{PT} is proposed to describe the impact of the local narrow trapped charges in SONOS memory. Program condition optimization, CHISEL program method and cell structure optimization, have been demonstrated to decrease the sub-threshold leakage current and improve the program characteristics.

Acknowledgements

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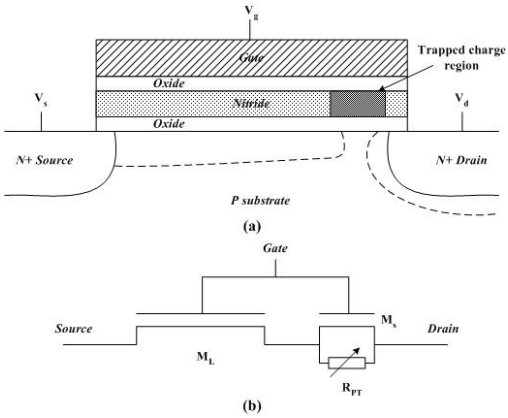

Fig.1. (a) Local-trapped charges in SONOS memory cell and (b) proposed model that contains two transistors and a changeable resistor.

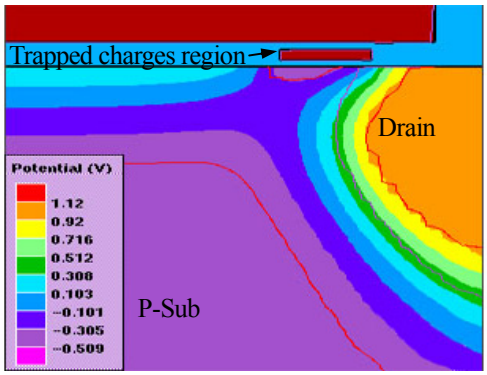

Fig.2. The potential distribution near the Drain side after program.

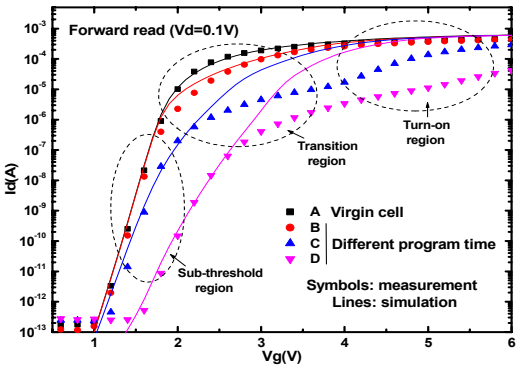

Fig.3. I_d-V_g characteristics of virgin cell (curve A), and programmed cell (curve B, C, D, refer to different program time). The symbols are measurement result, and lines are simulation result.

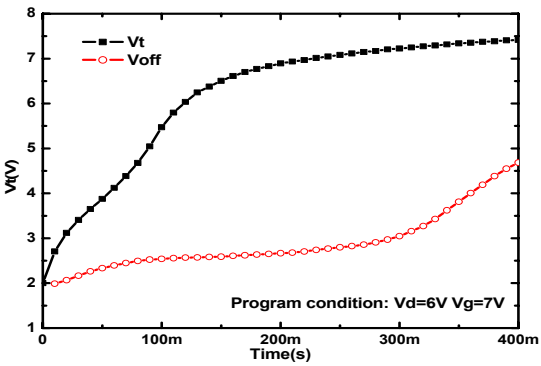

Fig.4. V_T and V_{off} during CHE programming.

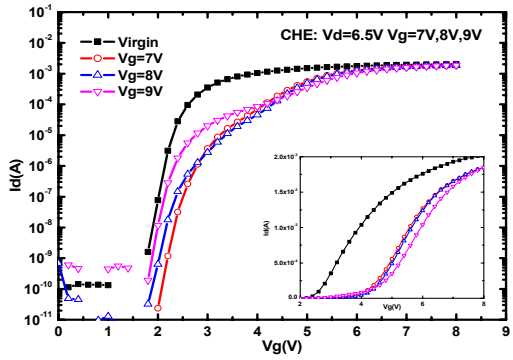

Fig.5. Comparison of different program Gate voltage of CHE (V_g=7V, 8V, 9V, separately). Inset illustrates the ID-VG curves in the linear coordinate.

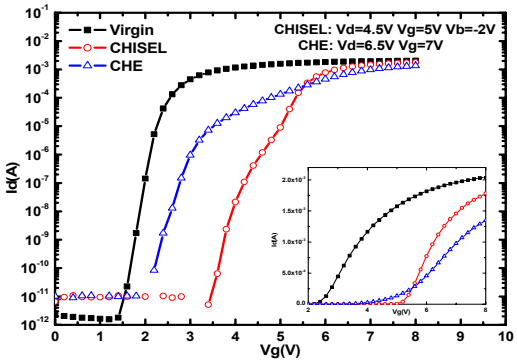

Fig.6. Comparison of CHISEL program and CHE program. Inset illustrates the ID-VG curves in the linear coordinate.

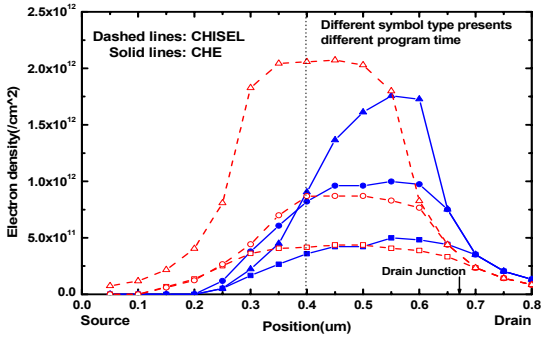

Fig.7. Trapped electron distribution after CHE or CHISEL program.

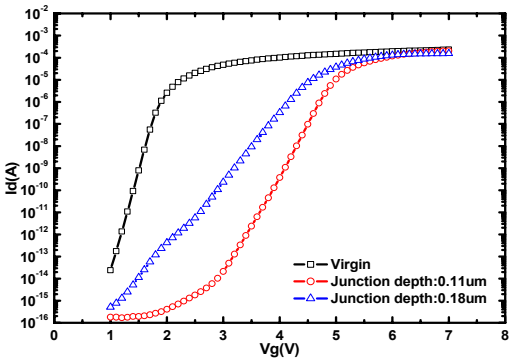

Fig.8. Simulation results of different junction depth of Drain.