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Low Voltage and High Speed Efficient Flash Using Band-to-Band Tunneling Induced Substrate Hot Electron Injection (BBISHE) to Perform Programming

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1. Introduction

NOR-type ETOX flash cells use channel hot electron injection (CHEI) for programming which features low voltage operation and high programming speed. However, the throughput for CHEI programming is low due to its low programming efficiency. Various innovations in cell structure or operation schemes such as, CHEI with substrate bias named CHISEL [1] or split-gate structure [2] are proposed to improve programming efficiency.

Band-to-Band tunneling induced substrate hot electron injection (BBISHE) is induced by the avalanche breakdown in the deep depletion region controlled by gate voltage. The band-to-band tunneling induced hot electrons are accelerated by the deletion region and directly inject into the gate. In previous reports, a long channel BBISHE mechanism was studied [3] [4]. In this work, a novel cell array using BBISHE programming with a divided p-substrate line and channel FN tunneling erasing is proposed to achieve high efficiency programming and high density array.

2. Cell Structure and Array

Fig. 1 shows the proposed the flash memory based on a ETOX flash cell with a higher p- threshold implantation. The sample devices with 100Å tunneling oxide and 170Å inter-poly dielectric (LP-CVD oxide) are fabrication with I-line lithography with channel length of 0.4μm. The p-sub lines separated by STI are necessary for realizing a NOR-type array shown in Fig. 2. Table I shows the proposed array operation condition.

3. Cell Operation and Characteristics

During the proposed BBISHE programming operation, the source line, bit line, word line and p-substrate line voltages are set to 0V, floating, 10V and -6.5V, respectively. The hot carrier generation mechanism is schematically illustrated in Fig. 1. Fig. 3 shows the I_D and I_{FG} versus the floating gate potentials at various substrate biases. Higher saturated I_{FG} is observed when the transistor operates in strong inversion region (V_{FG}>5V) because of the surface inversion layer prevents the banding in the p- substrate region. The I_{FG} is about 4nA/μm at V_{FG}=6V, V_B=-6.5V and V_S=0V. In the unselected cells with the same p-sub line, its drain leakage current and I_{FG} can be inhibited to less than 0.1nA/μm and 0.1pA/μm, respectively. Therefore, the p-sub line disturbance during programming is minimal. The programming efficiency (I_D/I_{FG}), shown in Fig. 4, ranges from 0.02 to 0.001 depends on whether the channel is formed. Fig. 5 compares the programming characteristics of the cells with the different threshold implant levels. With 0.4μm channel length, higher threshold implant dosage of $2x10^{13}cm^{-2}$ is needed for less than -7V substrate bias operation. Fig. 6 shows the programming characteristics of cells of different channel lengths. Because the BBISHE current is proportional to the active gate area, the same gate current density results in similar programming speed with different channel lengths.

Fig.7 shows the programming trends at different V_{CG}. Threshold voltage window of 4V is obtained within 10μs. Two programming modes are observed: first, when the cell is in strong inversion, highest I_{FG} for BBISHI is obtained. While the transistor is biased at deep-depletion mode, the BBISHE injection current is lower, hence, results in a smaller programming speed.

For this flash cell, channel FN tunneling is adopted for the erase operation. Fig. 8 exhibits the erase characteristics with the word line voltage of -9V~-11V, the p-sub line of 6V and floats the bit line and source line, where the erase time of less than 100ms is demonstrated.

The cells sharing the same word-line or p-sub line with the selected cells may suffer from disturbance stress. Fig. 9 shows the p-sub line and word line disturbance characteristics. No significant threshold voltage increment is observed by word line disturbance stress. The p-sub line disturbance is more severe. However, the cells sharing the same p-sub line with selected cell can still sustain more than 1000x p-sub line disturbance.

Fig. 10 shows the read disturbance characteristics. Under constant-voltage stress, V_D= 1V, V_{CG}=3.3V, on the cell in low Vt, a good read disturbance is demonstrated.

The threshold voltage window versus program/erase cycles is shown in Fig. 11. No significant threshold voltage window closing is observed up to $5x10^5$ P/E cycles. The slight migration of erase states after 10^4 P/E cycles is caused by the electrons trapped in the tunneling oxide during channel FN erasing operation.

4. Conclusions

In this work, a novel 0.4μm flash memory cell with BBISHI programming mechanism is proposed and fabricated. High programming speed of 10μs and high efficiency of 0.02 are demonstrated. Sufficient margin for word line and p-sub line disturbances and excellent endurance characteristics are achieved.

Acknowledgement

The authors would like to thank the engineers at the VLSI facilities of the Department of Electrical Engineering, National Nano Device Laboratory (NDL) for the help on processing and National Science Council (NSC) for funding the this project.

References

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Table I: Typical Operation Conditions

Mode	Bit line	Word line	Sub line	Source Line	Deep n-well
	select / unselect	select / unselect	select / unselect		
PGM	Float/Float	10V/0V	-6.5V/0V	0V	0V
ERS	Float/Float	-10V/0V	6V/6V	Float	Float
Read	1V/0V	3.3V/0V	0V/0V	0V	0V

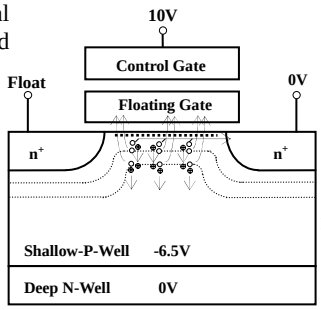

Fig. 1 Cell structure and schematic illusion of hot electron generation by BBISHE mechanism

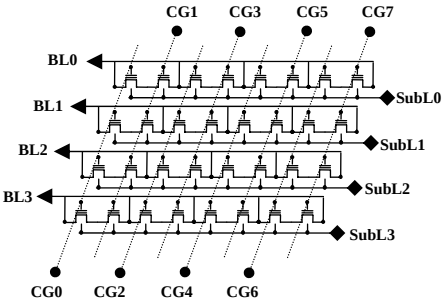

Fig. 2 Array architecture and the selective p- sub lines divided by STI

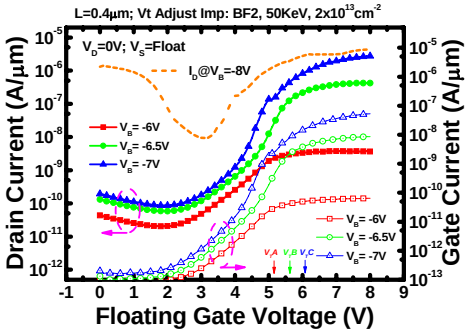

Fig. 3 The measured current spectrums with the different floating gate voltages.

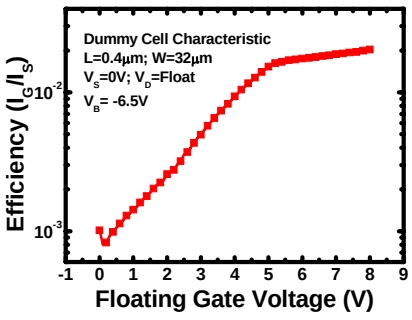

Fig. 4 The measured efficiency (I_G/I_S) of dummy cell during programming operation.

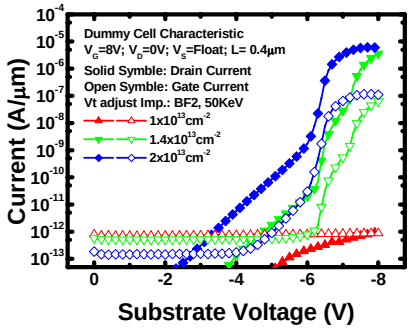

Fig. 5 The measured current spectrums with the different Vt adjust implantation splits.

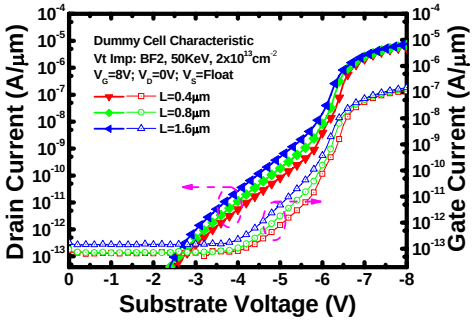

Fig. 6 The measured current spectrums with the different channel length.

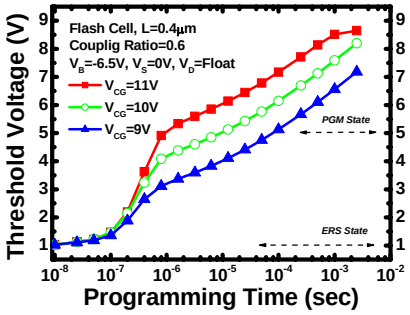

Fig. 7 Vt shift as a function of programming time for different control gate voltages.

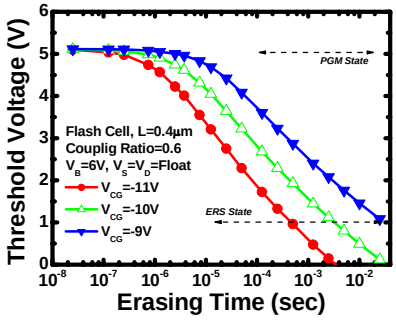

Fig. 8 Vt shift as a function of erasing time for different control gate voltages.

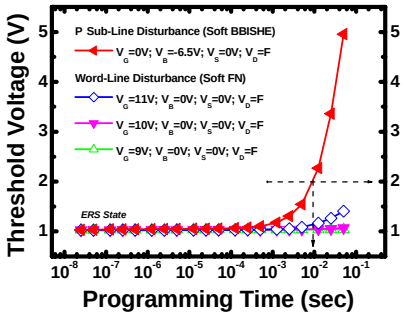

Fig. 9 The measured sub-line and word-line disturbance characteristics

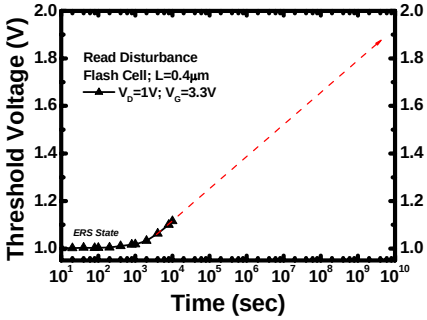

Fig. 10 The 10 years lifetime prediction of read disturbance characteristics.

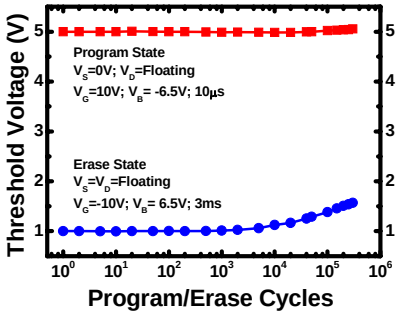

Fig. 11 Endurance Characteristics