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Reduced Hot-Carrier Induced Degradation of NMOS I/O Transistors with Sub-micron Source-Drain Diffusion Length for 0.11 μm Dual Gate Oxide CMOS Technology

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1. Introduction

The effect of reduced source-drain diffusion length (L_{ov}) on hot-carrier induced degradation of NMOS I/O transistors using 0.11 μm dual gate oxide (DGO) CMOS technology will be reported. An understanding of hot-carrier induced degradation would be very important for modern dual gate oxide (DGO) CMOS integrated circuits. As shown in Table I, the average electric field perpendicular to the channel (estimated from V_{dd}/T_{ox}) for both core and I/O transistors are similar, thus implying that the I/O transistors with the significantly higher supply voltage will suffer from more serious hot carrier degradation problems [1]-[3]. And since hot carrier degradation is usually more serious in NMOS transistors, we will focus our discussion on the effect of L_{ov} reduction on hot-carrier induced degradation in n-channel thick gate oxide I/O MOS transistors. It is discovered that as L_{ov} (definition shown in Fig. 1) decreases, which then gives rise to compressive strain in the channel region of the transistor, hot-carrier induced degradation in NMOS I/O transistors is reduced. Direct-Current Current-Voltage (DCIV) spectrum suggests that no additional interface traps (ΔN_{it}) generation or charge trapping were created when using shorter L_{ov}.

2. Experimental Setup

Device Fabrication

The *MOS* transistors under study were all fabricated with our 0.11 μm DGO *CMOS* design rule on 200 mm p-type *Si* wafers. The equivalent oxide thickness (EOT) measured from capacitance-voltage (C-V) measurements on a 100/100 μm capacitor was approximately 5 nm under inversion. Advanced features such as source-drain extension structures, halo/pocket implant, supersteep retrograde well, *L*-shaped spacers, cobalt salicide and shallow trench isolation (STI) were all adopted. It is important to note that for our STI step, a densification step using a temperature of ~1000 °C was used. The STI process flow used in this experiment is shown in Fig. 1. The drawn gate width (W_{drawn}) for all the transistors tested was 10 μm.

Device Characterization

The drain stress voltage (V_{dstr}) applied during the hot carrier stress ranged from +3.0 V to +4.0 V and the gate voltage (V_{gstr}) was chosen to maximize the substrate current ($V_{gstr} = V_{gs}@I_{submax}$). At this condition, the leakage current through the gate oxide is negligible.

3. Results and Discussions

Hot-Carrier Stress Results

The L_{ov} dependence of the threshold voltage (V_T) degradation, $\Delta V_T/V_{T0}$ with respect to stress time, is shown in Fig. 2. V_T is obtained using the constant current extraction method with the constant current being referenced at (W_{drawn}/L_{drawn})*0.1 μm. As the L_{ov} becomes smaller, $\Delta V_T/V_{T0}$ becomes smaller. The degradation improvement for smaller L_{ov} becomes more significant as the stress time becomes longer (in this case, >100 s). Figure 3 shows the I_{dlin} degradation for different L_{ov} where I_{dlin} refers to I_d when V_{gs} is 1.2 V and the corresponding V_{ds} is 0.05 V. Once again, it is obvious that shorter L_{ov} will lead to better reliability of NMOS transistors. It may be quite likely that the improvement in the reliability shown by Fig. 3 is a result of a reduction in additional N_{it} or interface trap generations caused by the compressive stress due to the proximity of STI to the channel region of the transistor. As such, we will be using the DCIV spectra to measure the relative change in N_{it}.

The Interface Trap Generation Measured by the DCIV Technique

Figure 4 shows the DCIV spectra for L_{ov} = 5 μm and L_{ov} = 0.31 μm. For both transistors, it can be seen that N_{it} will increase with increasing stress time. To investigate whether the different L_{ov} will lead to an increase in interface trap generation (ΔN_{it}), we will calculate $\Delta DCIV_{peak}$ where

$$\Delta DCIV_{peak} = DCIV_{peak} - DCIV_{peak0}.$$

The subscript "peak0" refers to the peak base current of the DCIV spectrum obtained at stress time = 1 s and the subscript "peak" refers to the peak base current of the DCIV spectrum at any particular stress time of interest. $\Delta DCIV_{peak}$ will allow us to derive the ΔN_{it} since the two terms are directly related. Figure 5, which is the graph of $\Delta DCIV_{peak}$ with respect to stress time, shows that for both L_{ov} values of 5 and 0.31 μm, there is no significant difference in $\Delta DCIV_{peak}$. We also used a higher V_{dstr} value of +4.0 V, and similar conclusions can be made. We therefore claim that additional mechanical stress, in this case due to the proximity of STI to the channel region, does not enhance or

increase the rate of interface trap generations. This result is similar to that obtained by Degraeve *et al*. [4], [5], in which compressive strain was deliberately introduced to the transistors by using a cantilever system and weights. We propose that the reduction of the hot-carrier induced degradation of NMOS transistors is due to a compressive strain generated when L_{ov} is reduced [6], [7], resulting in the suppression of hot electron generation due to the compressive strain according to the theory proposed by Degraeve *et al*. [4], [5].

4. Conclusions

We have found that the hot-carrier degradation of NMOS transistors is improved when we use a shorter L_{ov}. A shorter L_{ov} will correspond to additional mechanical stress due to the proximity of the STI to the channel region of the NMOS transistor. It was further discovered, using the DCIV spectra, that the additional mechanical stress will not enhance or increase ΔN_{it}. We therefore attribute the improvement in the hot-carrier induced degradation of NMOS transistors to be due to the suppression of hot electron generation due to the additional compressive strain.

References

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Table I: Comparison of core and I/O MOS transistors of 0.11 μm DGO CMOS technology

	Core	I/O
Gate Length (L_{gate})	0.11 μm	0.16 μm
Gate Oxide Thickness (T_{ox})	1.8 nm	5.0 nm
Supply Voltage (V_{dd})	1.0 V	2.5 V
V_{dd}/T_{ox}	0.56 V/nm	0.5 V/nm

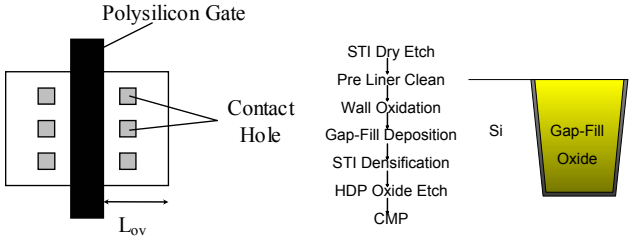

Fig. 1 Definition of L_{ov} and the process flow of STI step.

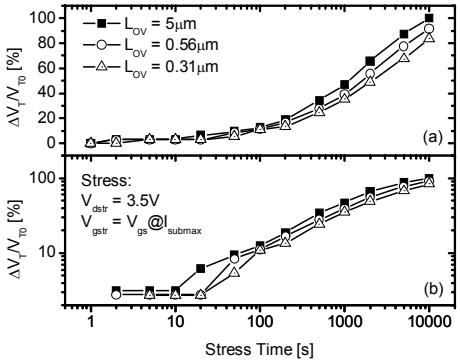

Fig. 2(a) Plot of $\Delta V_T/V_{T0}$ vs. stress time with $\Delta V_T/V_{T0}$ in linear scale for different L_{ov}. (b) Plot of $\Delta V_T/V_{T0}$ vs. stress time with $\Delta V_T/V_{T0}$ in logarithm scale for different L_{ov}.

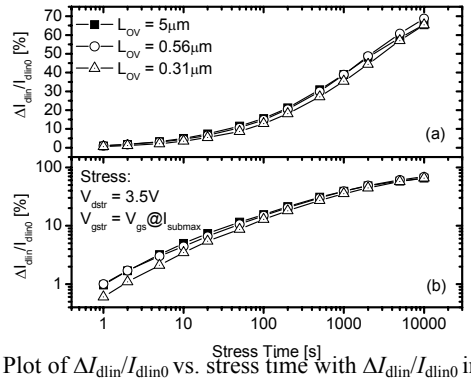

Fig. 3(a) Plot of $\Delta I_{dlin}/I_{dlin0}$ vs. stress time with $\Delta I_{dlin}/I_{dlin0}$ in linear scale for different L_{ov}. (b) Plot of $\Delta I_{dlin}/I_{dlin0}$ vs. stress time with $\Delta I_{dlin}/I_{dlin0}$ in logarithm scale for different L_{ov}.

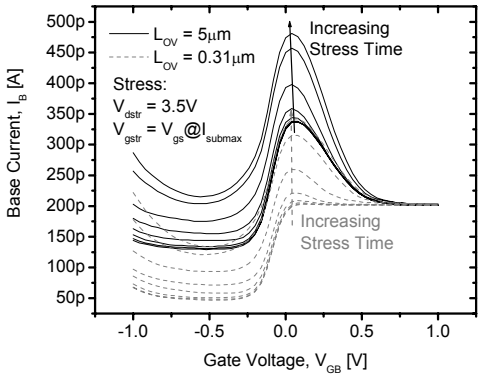

Fig. 4. DCIV spectra for L_{ov} = 5 μm and L_{ov}= 0.31 μm.

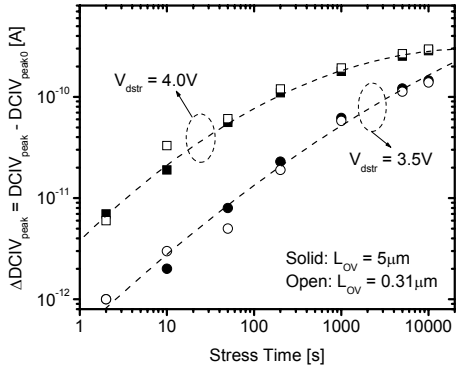

Fig. 5. $\Delta DCIV_{peak}$ in this plot is related to ΔN_{it}. For both L_{ov} values, it can be seen that $\Delta DCIV_{peak}$ almost coincides for different stress times and different V_{dstr} bias. This plot suggests that mechanical stress from STI does not enhance N_{it} generation.