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RTS amplitudes in decanano n-MOSFETs with conventional and high-κ gate stacks

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1. Introduction

Low frequency (LF) noise in MOSFETs has been a topic of interest to both academia and industry in recent years. It is becoming a major concern for analogue circuit performance [1], DRAM operation [2], and will eventually impact critically upon the reliability of digital logic especially as devices continue to scale towards smaller dimensions. Random Telegraph Signals (RTS) caused by the capture and emission of carriers in traps at the Si/SiO_2 interface have been posited as a major component of low frequency noise in semiconductor devices. 1/f noise can usually be described as a superposition of Lorentzian power spectra and amplitude fluctuations larger than 60% have been observed in a decanano MOSFETs at room temperature [3].

2. Simulation of RTS amplitudes

The change in the drain current associated with trapping events in defect states was investigated using 3D numerical simulations [4]. We have shown previously [5] that a trapped charge at the Si/SiO_2 interface results in a reduction in the nominal drain current due to the electrostatic influence of the trapped electron. This reduction in current is usually referred to as the RTS amplitude. The magnitude of the RTS amplitude is largest through the subthreshold region at the lower gate voltages. However, the amplitude reduces in the strong inversion region above threshold because the mobile charge in the inversion layer increasingly screens out the electrostatic influence of the trapped charge [5].

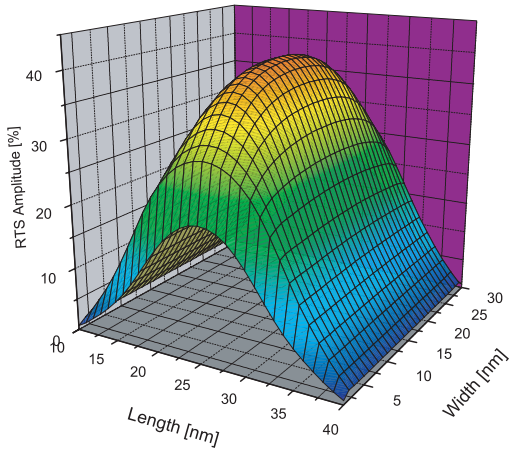

Figure 1. Dependence on trap position within the channel of RTS fluctuations in the drain current of a 30×30nm MOSFET.

Figure 1 presents the dependence of the RTS amplitude on the location of the trapped charge within the channel of a 30×30nm MOSFET. The RTS amplitude reaches its peak at the centre of the channel where the charge has a strong localised effect on the height of the source-to-drain barrier which is illustrated in Figure 2. When the trapped charge is placed in the vicinity of the source and drain it has virtually no effect on the drain current as the large concentration of mobile carriers present in the highly doped source/drain tends to screen out the trapped charge.

Figures 3 and 4 illustrate the dependence of the relative RTS amplitude on gate voltage for 30 nm n-channel devices with different oxide thicknesses. The single trapped charge

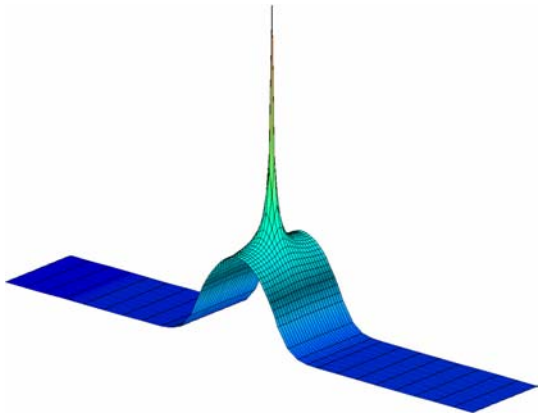

Figure 2. The potential barrier between source and drain in a MOSFET, and the effect on this of a single trapped electron in the centre of the channel located at the Si/SiO_2 interface.

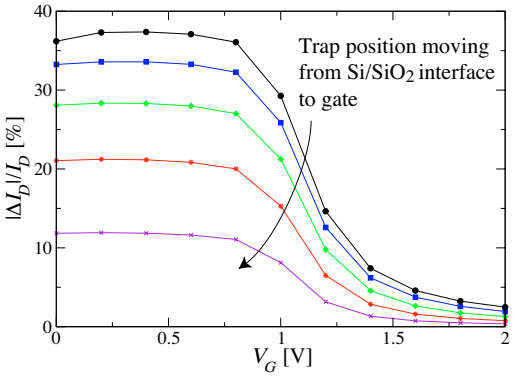

Figure 3. Relative RTS amplitudes for a 30 nm n-channel MOSFET with oxide thickness, t_{ox}=3nm, for a trap at different positions within the oxide. A metal gate is assumed.

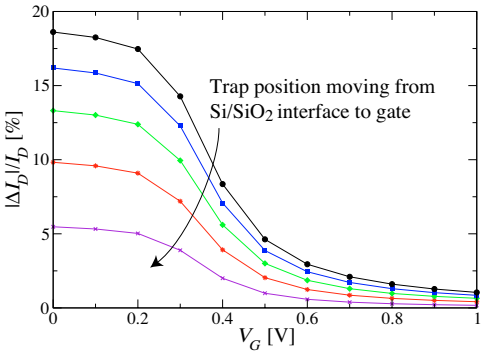

Figure 4. Relative RTS amplitudes for a 30 nm n-channel MOSFET with oxide thickness, t_{ox}=1nm, for a trap at different positions within the oxide. A metal gate is assumed.

is placed in the middle of the channel producing the largest RTS amplitude. For each curve the vertical position of the trapped charge within the oxide is changed, moving from the Si/SiO_2 interface to the gate. The device simulated for Figure 3 has oxide thickness t_{ox}= 3 nm, while the results in Figure 4 are for a device with t_{ox}= 1 nm. These results follow the same trend observed in Figure 1. As the location of the trapped charge moves towards the gate the electrostatic effect on the channel potential is reduced, hence the RTS amplitude is lower. The thinner oxide in Figure 4 has the effect of reducing the magnitudes of the RTS amplitudes. The closer proximity of the gate to the channel can more efficiently screen the effect of the trapped charge, smoothing the electrostatic potential within the channel.

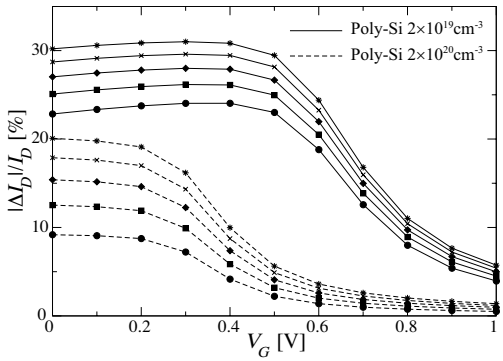

Figure 5. Relative RTS amplitudes for a 30 nm n-channel MOSFET with oxide thickness, t_{ox}=1nm, for a trap at different positions within the oxide. Two different dopings of poly-Si gate are shown.

Figure 5 presents results for the simulations similar to those in figure 4, except that the metal gate has been replaced with a poly-silicon gate. Results for two different poly-silicon gate dopings, 2 10^{19}cm^{-3} and 2 10^{20}cm^{-3}, are shown. The low doping concentration is chosen to highlight the effect of poly-Si depletion. With a poly-Si doping of 2 10^{20}cm^{-3} the RTS amplitudes are similar, but slightly different to those with a metal gate. With the lower poly-Si doping the depletion layer at the gate/oxide interface is wider, thus reducing the screening from the mobile electrons in the gate. This leads to higher RTS amplitudes.

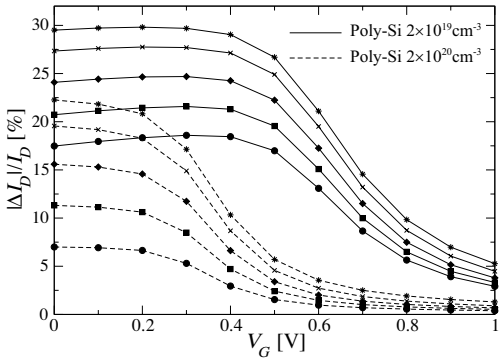

Figure 6. Relative RTS amplitudes for a 30 nm n-channel MOSFET with high-κ dielectric thickness, t_{ox}=5.64nm, for a trap at different positions within the oxide. Two different dopings of poly-Si gate are shown.

The simulations for Figure 5 were repeated for a device with high-κ dielectric (HfO_2) with the same equivalent oxide thickness. The relative permittivity ε_{HfO2}=22 and oxide thickness t_{ox}= 5.64 nm. The results are shown in Figure 6. For a trap at the Si/HfO_2 interface (the curves with the highest amplitudes in each case) the results are the same as in the device with SiO_2 gate insulator. However, as the position of the trap gets closer to the gate the reduction in amplitude is more pronounced in the high-κ case.

3. Conclusions

3D numerical simulations have been performed to calculate RTS amplitudes due to electrons caught in traps within the oxide of decananometre MOSFETs. The position of the trap within the oxide has been investigated and shown to greatly affect the RTS amplitudes. We have also shown that the use of a poly-silicon gate results in higher amplitudes associated with reduced screening due to the poly depletion layer. Similar results are also observed when the SiO_2 in the simulations is replaced with a high-dielectric.

References

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