1. Introduction

Low frequency (LF) noise in MOSFETs has been a topic of interest to both academia and industry in recent years. It is becoming a major concern for analogue circuit performance [1], DRAM operation [2], and will eventually impact critically upon the reliability of digital logic especially as devices continue to scale towards smaller dimensions. Random Telegraph Signals (RTS) caused by the capture and emission of carriers in traps at the Si/SiO$_2$ interface have been posited as a major component of low frequency noise in semiconductor devices. 1/f noise can usually be described as a superposition of Lorentzian power spectra and amplitude fluctuations larger than 60% have been observed in a decanano MOSFETs at room temperature [3].

2. Simulation of RTS amplitudes

The change in the drain current associated with trapping events in defect states was investigated using 3D numerical simulations [4]. We have shown previously [5] that a trapped charge at the Si/SiO$_2$ interface results in a reduction in the nominal drain current due to the electrostatic influence of the trapped electron. This reduction in current is usually referred to as the RTS amplitude. The magnitude of the RTS amplitude is largest through the subthreshold region at the lower gate voltages. However, the amplitude reduces in the strong inversion region above threshold because the mobile charge in the inversion layer increasingly screens out the electrostatic influence of the trapped charge [5].
is placed in the middle of the channel producing the largest RTS amplitude. For each curve the vertical position of the trapped charge within the oxide is changed, moving from the Si/SiO$_2$ interface to the gate. The device simulated for Figure 3 has oxide thickness $t_{ox} = 3$ nm, while the results in Figure 4 are for a device with $t_{ox} = 1$ nm. These results follow the same trend observed in Figure 1. As the location of the trapped charge moves towards the gate the electrostatic effect on the channel potential is reduced, hence the RTS amplitude is lower. The thinner oxide in Figure 4 has the effect of reducing the magnitudes of the RTS amplitudes. The closer proximity of the gate to the channel can more efficiently screen the effect of the trapped charge, smoothing the electrostatic potential within the channel.

The simulations for Figure 5 were repeated for a device with high-$\kappa$ dielectric (HfO$_2$) with the same equivalent oxide thickness. The relative permittivity $\varepsilon_{HfO_2}=22$ and oxide thickness $t_{ox}=5.64$ nm. The results are shown in Figure 6. For a trap at the Si/HfO$_2$ interface (the curves with the highest amplitudes in each case) the results are the same as in the device with SiO$_2$ gate insulator. However, as the position of the trap gets closer to the gate the reduction in amplitude is more pronounced in the high-$\kappa$ case.

3. Conclusions

3D numerical simulations have been performed to calculate RTS amplitudes due to electrons caught in traps within the oxide of decananometre MOSFETs. The position of the trap within the oxide has been investigated and shown to greatly affect the RTS amplitudes. We have also shown that the use of a poly-silicon gate results in higher amplitudes associated with reduced screening due to the poly depletion layer. Similar results are also observed when the SiO$_2$ in the simulations is replaced with a high-dielectric.

References