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65nm-node Low-Standby-Power FETs with HfAlOx Gate Dielectric

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1. Introduction

Development of high-k gate dielectrics has recently been accelerated for the purpose of introducing them to 65nm-node low-standby-power (LSTP) devices whose mass production is scheduled in 2007[1].
HfAlOx is one of the promising candidates because of its high crystallization temperature (>1050 ^{o}C) and moderate dielectric constant. However, Hf-based high-k gate stacks have two big issues [2], *i. e.*, the mobility degradation due to residual impurities incorporated in the films and threshold voltage (Vth) shifts due to the interaction between high-k film and poly-Si gate electrode.

In this study, we have investigated the relationship between transistor characteristics and process parameters of HfAlOx gate stacks from the viewpoint of device performances. By suppressing the mobility reduction and Vth shifts, high Ion, low Ioff and low gate leakage current suitable for LSTP application was successfully acchieved.

2. Fabrication Process

CMOS FETs with HfAlOx gate dielectrics were fabricated using advanced dual gate process, as shown in Table 1. After shallow trench isolation (STI) formation and channel implantations, a nitrided interfacial layer (SiON-IL) was intentionally formed by NH_3 nitridation and re-oxidation [3]. HfAlOx film was deposited by ALD at 300^{o}C and Hf concentration (Hf/Hf+Al) was set to be 30 %. TEMAHf ($Hf(NEtMe)_4$) or hafnium tetrachloride ($HfCl_4$) was used as a precursor for HfO_2 layer [4]. Post-deposition annealing was done at 1000^{o}C. A 150 nm-thick poly-Si film was deposited by low temperature deposition method at 590^{o}C [5], followed by n/p-gate implantations and gate electrodes patterning. After S/D extension and halo implantations, SiN sidewall was formed followed by deep S/D implantations. Implanted impurities were activated by spike annealing at 1000^{o}C. NiSi salicidation was used to ensure the high drive currents by reducing the S/D sheet resistance. Figure 1 is a cross-sectional TEM photograph showing the fabricated FET with gate length of 60 nm.

3. Results and Discussions

Gate Dielectric integrity

Firstly, the influence of residual impurities in HfAlOx films on the film properties was investigated. The gate leakage current (Jg) dependence on equivalent oxide thickness (EOT) is shown in Fig. 2. By using the TEMAHf as a Hf precursor and by applying NH_3 plasma pulse just after the HfO_2 layer formation, the amount of radical impurity can be reduced to be 1/5 [4]. As a result, Jg was reduced two orders of magnitude as compared with that of $HfCl_4$ based HfAlOx. The electron mobility was also improved by 20 %, as shown in Fig. 3.

Secondary, the influence of nitrogen concentration [N] in SiON-IL was investigated. Figure 4 shows Id-Vg characteristics for n and pFETs with various nitride concentrations in the IL. If the nitrogen concentration in the IL is too high ($[N]_{peak}$>30%), positive charges inherent to the Si-N bond cause negative shift in the Vth (0.3 and -0.8 V for n- and pFETs, respectively). Reducing the nitrogen concentration to be about 15 at%, the Vth values of 0.6/-0.5V (n/p), which were suitable for the 65 nm-node LSTP applications, were obtained. Note that these Vth values were achieved without counter implantation. By eliminating the positive charges due to the excess nitrogen, hole mobility was improved about 40%, as shown in Fig. 5.

Finally, we tried to optimize the IL thickness to improve FET's performances. The mobility reduction can be suppressed by making the IL thickness large because the scattering center is separated from the channel. Figure 6 shows the relationship between EOT and IL thickness (the optical thickness before HfAlOx deposition). HfAlOx thickness was fixed to be 1.2nm in this experiment. In order to make the EOT less than 1.5nm, IL thickness can be as large as 1.9nm. Using the 1.6nm-thick IL, the electron mobility is drastically improved up to 50 %, as shown in Fig. 7. The relationship between IL thickness and mobility, Ion and EOT are summarized in Fig. 8. When IL is too thin, boron penetration occurred, resulting in the degradation in pFET properties. On the other hand, when IL is too thick, EOT increases, leading to Ion reduction. According to this figure, the 1.3 nm-thick IL was selected.

CMOS Performance

The FET properties were much improved by reducing the residual impurities in HfAlOx film and employing the optimized IL, together with channel engineering. The sub-threshold characteristics are shown in Fig.9. Good S-factors of 76 and 86 mV/decade have been obtained for nFETs (Lg=90 nm) and pFETs (Lg=60 nm), respectively. The leakage currents are well suppressed and a good balance of Ig and Isub has been achieved. Figure 10 shows the Vth roll-off characteristics. Almost symmetrical Vth values of 0.4 V and -0.5 V, which is suitable for LSTP application, have been obtained for n and pFETs. Figure 11 shows Ion-Ioff characteristics at 1.1 V supply voltage. Sufficiently high Ion values of 360 and 150 μA/μm have been achieved for nFETs (Lg=90 nm) and pFETs (Lg=60 nm), respectively at Ioff=20 pA/μm.

4. Conclusions

The effects of the residual impurities and interfacial layer on the characteristics of FETs with HfAlOx gate stacks have been studied. Residual impurity reduction enables gate leakage reduction of two orders of magnitude. By optimizing the thickness and nitrogen concentration of interfacial layer, good mobility and suitable threshold voltages have been obtained without counter implant. We have successfully fabricated CMOSFETs with HfAlOx gate dielectric for 65nm-node LSTP applications, Ion of which is 360 and 150 μA/μm for nFETs(Lg=90 nm) and pFETs (Lg=60 nm), respectively at Ioff=20 pA/μm at Vd=1.1 V.

References

[1] International Technology Roadmap for Semiconductors 2003.
[2] C.Hobbs et al., Tech. Dig.VLSI Symp, p. 9, 2003.
[3] R. Mitsuhashi et al., Ext. Abst.51st Spring Meeting of JSAP, (2003) p.885
[4] T. Kawahara et al., Extended.Abstracts.IWGI, p. 32. 2003
[5] A. Muto et al., Ext. Abst.51st Spring Meeting of JSAP, (2003) p.860

Table 1. Fabrication flow for HfAlOx FETs

STI
Channel I / I
Gate Dielectric
IFL Nitridation / IFL Re-Oxidation
HfAlOx Deposition (ALD)
PDA 1000C 1sec
GatePoly-CVD - PolySi
Gate-I / I
Annealing
Extension - I / I
Side Wall Depo & EB
S / D - I / I
Annealing (Activation 1000C)
Metalization

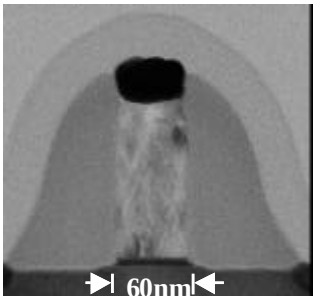

Fig.1 Cross-sectional TEM image of HfAlOx FET.

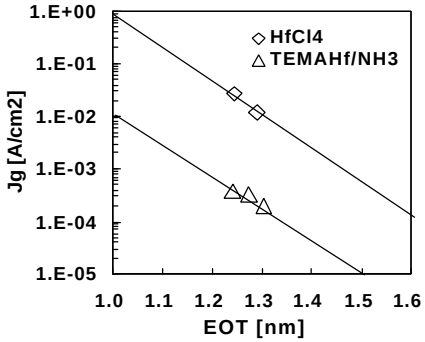

Fig.2 Relationship between EOT and Jg,which depends on the precursors of HfAlOx films.

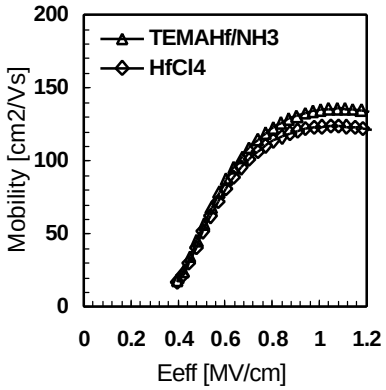

Fig.3 Electron Mobility dependence on the precursors of HfAlOx films.

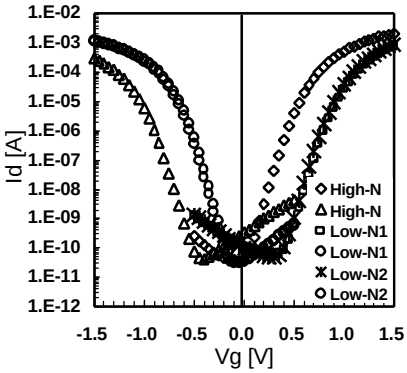

Fig.4 Id-Vg characteristics for n and pFETs, which depends on the nitride-concentration in IL.

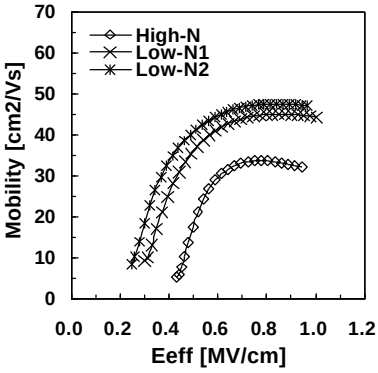

Fig. 5. Hole Mobility dependence on the nitride-concentration in IL.

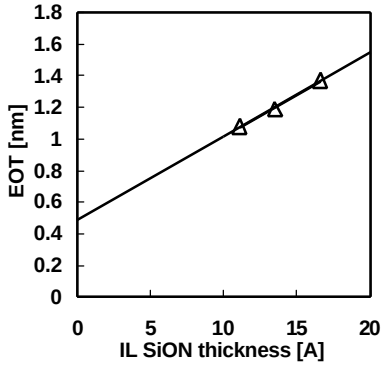

Fig.6 Relationship between EOT and IL SiON thickness.

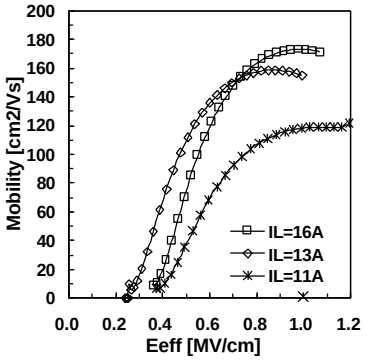

Fig. 7. Electron Mobility dependence on the thickness of IL SiON.

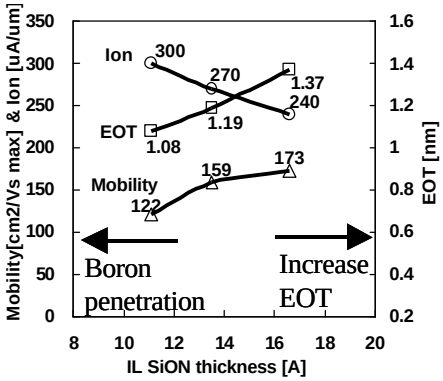

Fig.8 Relationship between IL thickness and Electron Mobility,Ion,and EOT.

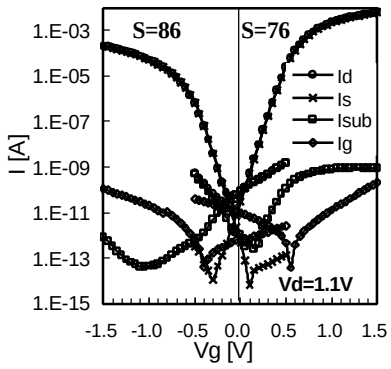

Fig. 9. Id-Vg characteristics for n and pFETs with W/L=10/0.09 um (N) and 10/0.06 um (P) at Vd=1.1V.

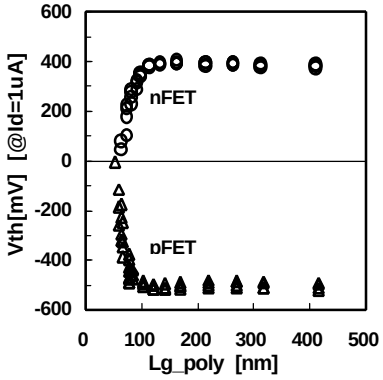

Fig. 10. Relationship between gate poly length and threshold voltage for n and p FETs with HfAlOx /SiON gate dielectric.

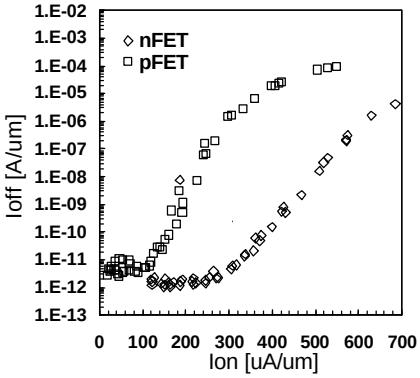

Fig. 11. Relationship between Ion and Ioff for n and p FETs with HfAlOx /SiON gate dielectric.