Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 430-431

P2-14

Dependence of Analog and Digital Performances on Mechanical Film Stress of ILD Layer in Nano-Scale CMOSFETs

S. H. Park, H. H. Ji*, Y. G. Kim*, H. D. Lee*, S. H Baek, K. C. Kim, B. S. Song,
H. K. Bae, H. S. Lee, Y. S. Kang, D. B. Kim, and J. W. Park

System IC PD Center, Hynix Semiconductor Inc., Hungduk-gu, Cheongju, Choongbuk, 361-725. Korea
Phone: +82-43-270-4452 E-mail: seonghyung.park@hynix.com
*Dept. of Electronics Engineering, Chungnam National University, Yusong-Gu, Daejeon, 305-764, Korea

1. Introduction

Due to the continuous scale-down of CMOS devices to nano-scale region, the integration of analog circuits along with digital circuits on a chip is becoming more and more important for mixed signal and/or SOC (System On Chip) applications. Therefore, concurrent improvement of analog and digital performances of nano-scale CMOSFETs is highly necessary for high performance and high density ULSI circuits [1]-[2]. And, there were report that the device performance of small geometry MOSFET is affected by the stress induced by shallow trench isolation and CVD films [3]-[5], However, the stress effect on the digital performance and analog performance were not considered concurrently.

In this paper, different dependence of NMOS and PMOS performance on the film stress is characterized in depth. Then, proposed herein is a method which can improve overall chip performance by controlling the stress of thin films such as silicide blocking layer and ILD layer.

2. Experiments

Figure 1 shows the process flow for experiments. After formation of and the source and drain, various silicide blocking layers (SBL) with different mechanical stress were deposited as a 1st split. Then, as a 2nd split, several inter-layer dielectric (ILD) layers with different mechanical stress were deposited after applying Co-silicide process.

The output resistance, Rout defined as (1) [6], and on current vs. off current are considered for representation of analog and digital performance, respectively. Figure 2 shows the measured voltage gain at different gate voltage. The voltage gain defined as (2). It is found that maximum DC gain is obtained at Vgs-Vth=0.2V point. Therefore, from now on, Rout and Ao will be evaluated at Vgs-Vth=0.2V.

$$Rout = \frac{\partial V_{ds}}{\partial I_{ds}} = \frac{1}{g_{ds}} \quad (1)$$

$$Ao = g_m \cdot R_{out} \quad (2)$$

3. Results and Discussion

The dependence of digital performance, i.e., Idsat vs. Ioff of CMOSFET on the silicide blocking layers is shown in Fig. 3 and 4. The film stress of BLC layer is summarized in Table I. The O3-USG with tensile stress shows the best NMOS digital performance than the others. Figure 5 also shows improved Rout characteristics of O3-USG case. These results show that the tensile stress improves not only digital performance but also analog performance of NMOSFETs. Although HLD layer also has tensile stress as in Table I, both the digital and analog performances were more degraded than LT-Ox with compressive stress, which is believed to be mainly due to the enhanced short channel effect by high processing temperature of HLD. However, in case of PMOS there is little difference of digital (Fig. 4) as well as analog (not shown here) performance between the films. Therefore, in case of silicide blocking layer, low thermal process with tensile film is desirable for improved NMOS performances. However, as shown in Fig. 3 and 4, the dependence of NMOS and PMOS on the film stress is not symmetry. Therefore, film stress should be optimized for overall improvement of NMOS and PMOS performances.

Table I. Stress status of thin films used for experiment. (dyne/cm^2)

	O3-USG	LT-Ox	HLD
Stress	6.1×10^8	-1.3×10^9	9.8×10^8
Status	Tensile	Compressive	Compressive

In case of ILD film, dependence of device performance on film stress is almost the same to SBL case. For example, the digital and analog performance of NMOSFET with PE-Nit layer (tensile stress) shows better performance then SiON (compress stress) as in Fig. 6. For exact analysis of performance dependence on the film stress, we used only PE-Nit BLC layer with different stress status. Figures 7~10 show the results of these experiments on the digital and analog performances of NMOS and PMOS. As we expected, the tensile stress improved a lot the digital and analog performance of NMOSFET. In case of PMOS, device dependence on the stress is less than NMOS and especially the analog performance shows little dependence on the stress although digital performance improved a little. It is said that tensile stress and compressive stress increase electron and hole mobility, respectively [5]. Electron and hole mobility dependence on ILD film stress show quite strong agreement with previous result as shown in Fig. 11. Fig. 12 depicts the stress effect of ILD film, i.e., ILD film with tensile stress make channel region tensile. Therefore, the film stress should be modified according to the bottleneck performances for high performance mixed and/or SOC application. For example, if NMOS and analog performance are of concern, the silicide blocking layer with tensile stress and ILD layer with no stress are desirable. If PMOS performance is bottleneck, compressive stress with SiON should be chosen with a little sacrifice with PMOS performance.

4. Conclusion

It is shown that the mechanical stress induced by the CVD process affects the digital and analog performance of CMOSFETs. The digital and analog characteristics show the

same trend for film stress while the performances of NMOSFET and PMOSFET show the trade-off. It is necessary to optimize the performance of NMOSFET and PMOSFET or analog and digital by controlling the mechanical film stress in nano-scale CMOS technology.

Acknowledgment

This work is supported in part by the National Program for Tera-level Nanodevices of the Ministry of Science and Technology as one of the 21 century Frontier Program.

References

[1] E. Morifuji et al., IEDM Tech. Digest, pp459-462, 2000
[2] A. Chatterjee et al., Symp. VLSI Tech. pp147-148, 1999
[3] Gregory Scott et al., IEDM Tech. Digest, pp827-830, 1999
[4] Y. G. Wang et al., IEEE Trans Electron Device, vol.50, p.529-531, February 2003
[5] Shin Ito et al., IEDM Tech. Digest, pp247-250, 2000
[6] J. H. Huang et al., IEDM Tech. Digest, pp569-572, 1992

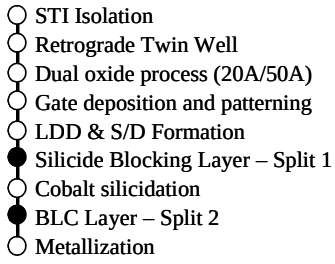


Fig. 1. Process flow for experiments. Solid circles show the split point.

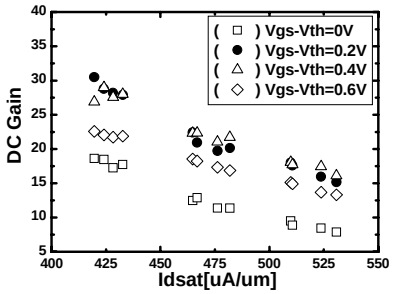


Fig. 2. Gain vs. Idsat characteristic as a function of Vgs - Vth.

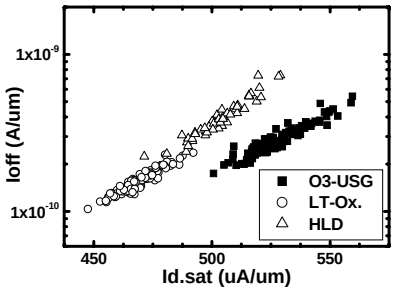


Fig. 3. Dependence of Idsat vs. Ioff characteristics of NMOSFET on the film stress of SBL layers.

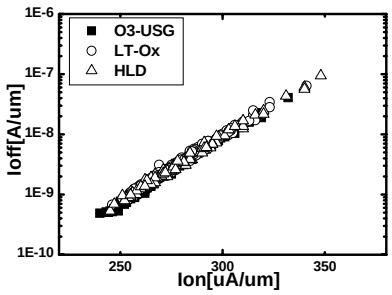


Fig. 4. Dependence of Ion vs. Ioff characteristics of PMOSFET on the film stress of SBL layers.

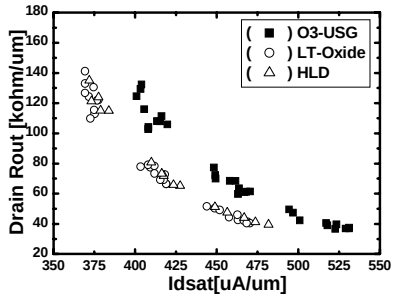


Fig. 5. Rout vs. Idsat of NMOSFET characteristic with different SBL layers.

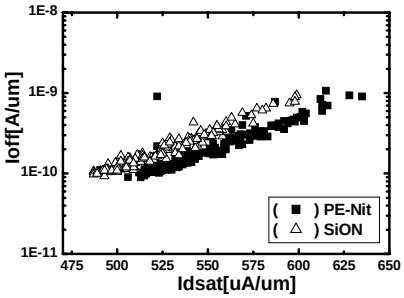


Fig. 6. Idsat vs. Ioff of NMOSFET with opposite mechanical stress type of ILD layers.

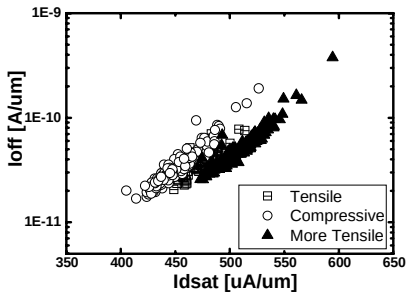


Fig. 7. Idsat vs. Ioff of NMOSFET with different mechanical stresses of PE-Nit ILD layer.

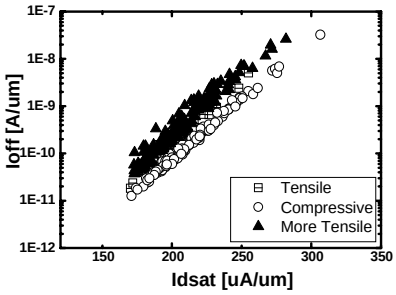


Fig. 8. Idsat vs. Ioff of PMOSFET with different mechanical stresses of PE-Nit ILD layer.

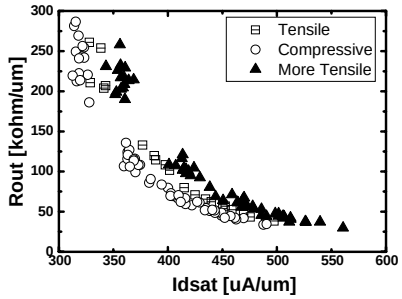


Fig. 9. Rout vs. Idsat of NMOSFET with different mechanical stresses of PE-Nit ILD layer.

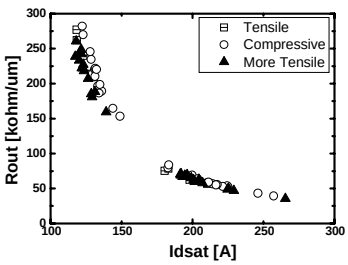
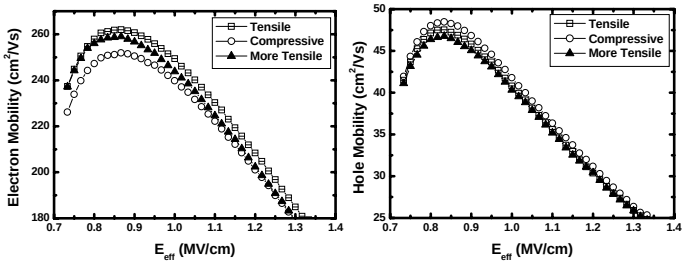


Fig. 10. Rout vs. Idsat of PMOSFET with different mechanical stresses of PE-Nit ILD layer.



(a) (b)

Fig. 11. (a) Electron and (b) Hole Mobility with different mechanical stresses of PE-Nit ILD layer.

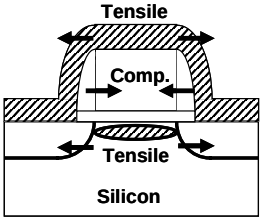


Fig. 12. Schematic cross-section showing the stress mechanism of the ILD layer.