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Damascene Gate CMOSFETs with 30 nm-Scale Gate Length

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Introduction

Although the planar MOSFET device has been the dominant structure for a few decades, its scaling becomes more and more difficult in sub-50 nm regime because of the rigorous requirements for gate oxide, gate patterning, lateral junction abruptness, S/D (Source/Drain) resistance, and poly depletion[1]. As one of the approach to overcome those problems, damascene gate scheme can be adopted[2]. The damascene gate process has many benefits over the conventional one such as easy gate length reduction using sidewall technique, sharp junction abruptness due to local channel implantation, easy implementation of recessed channel and metal gate, and so on[3-4].

In this paper, we demonstrate the ultimately scaled damascene gate CMOSFETs with sub-30 nm gate length fabricated by using 100 nm technologies.

Experimentals

Process sequence for the fabrication of damascene gate MOSFET is shown in Fig. 1. Silicon wafers are prepared with conventional trench isolation (STI) with HDP gap-fill. After pad-oxide/SiN/HDP stack deposition on top of the trench isolated silicon substrate, damascene gate patterns are formed by controlling the gate length with the spacer nitride thickness. Before the gate dielectric and poly-silicon gate stack deposition, boron and indium for NMOS and phosphorus and arsenic for PMOS are implanted through the open window of the gate patterning for the punch-through prevention and threshold voltage adjustment as local channel implantation (LCI). After sacrificial oxide layer removal, 1.2 nm oxynitride layer is used to gate dielectrics. Post-anneal treatment is applied with N_2 gas. Spike RTA (Rapid Thermal Anneal), Co salicide, low energy implantation, and low temperature single wafer oxide and SiN deposition processes are used to get the low resistivity of the gate and S/D as well as the shallow junction depth control. After the strip of SiN block surrounding the gate in H_3PO_4, the remained process is almost the same to that of conventional planar MOSFET.

Results and Discussion

Figs. 2 and 3 show the cross sectional TEM images for NMOS and PMOS transistors after their fabrication. The gate height and gate length (Lg) are 1130 nm and 25 nm for NMOS and 1350 nm and 35 nm for PMOS, respectively. Each gate profile has reverse trapezoid shape, which can play a role of offset spacer of 6 nm and 10 nm per side for NMOS and PMOS, respectively. Physical oxynitride thickness is 1.5 nm. Fig. 4 shows outstanding Vt roll-off characteristics. With damascene gate process, it is possible to extend the Vt roll-off down to 30 nm Lg with good SCE immunity. Fig. 5 shows the DIBL characteristics with various Lg for NMOS and PMOS, which shows that the short channel effects can be effectively suppressed with LCI and reduced halo implantation down to 40 nm Lg. Id vs. Vd and Id vs. Vg characteristics for a CMOSFET with the 30 nm-scale gate length shown in Figs. 6 and 7, respectively. They shows similar characteristics with previous data reported in the Lg=30 nm regime. At Vg=Vd=1.0 V, I*dsat* is 556 μA/μm for NMOS and 327 μA/μm for PMOS, respectively. Figs. 8 and 9 exhibit the C*j* of NMOS and PMOS with damascene gate scheme compared to conventional transistor scheme. Owing to LCI process, C*j* is reduced by 23% for NMOS and by 11% for PMOS, respectively. Using damascene gate process with LCI, we could place the channel implantation only under the gate region away from the S/D extension region where the dopant concentration is as high as the channel counter dopants. Therefore, the difficulties of large-tilted angle implantation as the patterns scale down below 50 nm would be replaced by low dose pocket implantation using this process, and C*j* can be reduced by LCI. Fig. 10 shows Vt controllability with vertical and lateral junction profile. Lateral graded profile is more important to effectively suppress SCE than vertical junction depth. In Fig. 11, Ion vs. Ioff characteristics for various Lg show that damascene gate scheme with LCI can be highly manufacturable and reliable in sub-30 nm regime.

Conclusions

In order to realize extremely scaled CMOSFETs, we have demonstrated damascene gate scheme process with local channel implantation. Owing to the merits of damascene gate process, 30 nm-scale CMOSFETs with the improved threshold voltage roll-off characteristics and short channel effect could be easily implemented. Also, junction capacitance reduced by 23 % for NMOS and by 11 % for PMOS, respectively. Thus, the scaling limit of planar CMOSFET can be also extended down to 30 nm gate lengths by using damascene gate process without complicated schemes.

References

[1] L. Chang, *et al.*, *Proc. of the IEEE*, Vol. 91, No. 11, p. 1860, 2003.
[2] C.-P. Chang, *et al.*, *Tech. Dig. of IEDM '00*, p. 53, 2000.
[3] C. W. Oh, *et al.*, *Tech. Dig. of VLSI Tech.'03*, p. 147, 2003.
[4] J. D. Choe, *et al.*, *IEEE Elec. Dev. Lett.*, Vol. 24, p. 195, 2003.

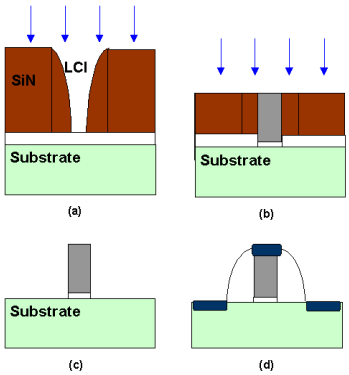

Fig. 1. Damascene process sequence. Local channel implantation is applied only in the channel region.

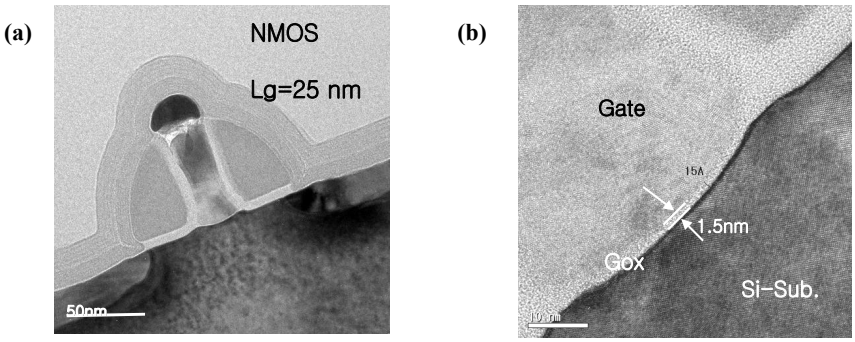

Fig. 2. TEM images for (a) NMOS with Co-salicided gate and source/drain. The physical gate length is 25 nm. (b) Gate dielectric is oxynitride with 1.5 nm physical thickness.

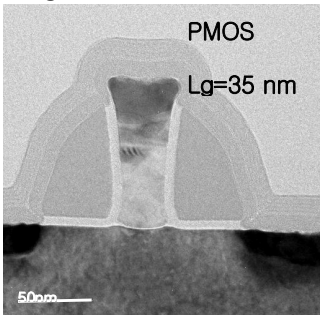

Fig. 3. TEM image of PMOS with 35 nm gate length. Gate profile is reverse trapezoid shape.

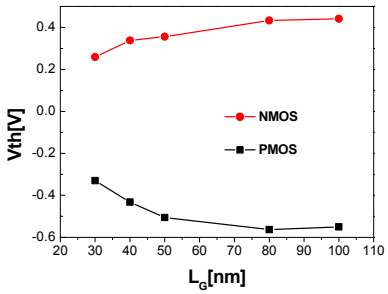

Fig. 4. Vt roll-off characteristics of NMOS and PMOS. Damascene gate process gives Vt controllability down to 30 nm Lg.

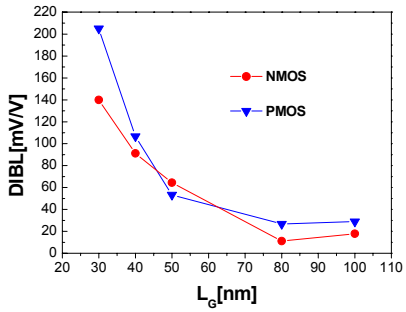

Fig. 5. DIBL characteristics depending on various Lg for NMOS and PMOS. LCI can improved the DIBL characteristics.

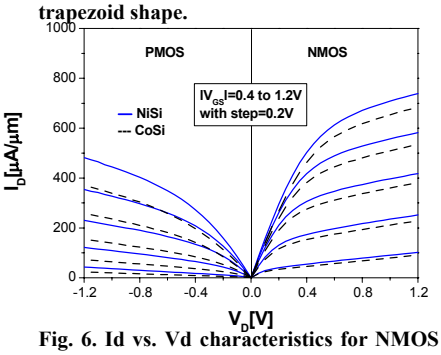

Fig. 6. Id vs. Vd characteristics for NMOS and PMOS with 30 nm Lg. Ni-salicide is more attractive than Co-salicide in the Lg=30 nm regime. Idsat is 509 μA/μm and 556 μA/μm for NMOS, respectively, at Vg=Vd=1.0 V.

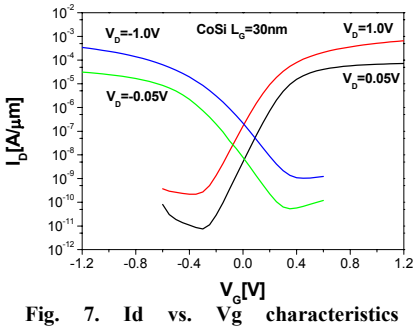

Fig. 7. Id vs. Vg characteristics of NMOS/PMOS with 30 nm-scale Lg. DIBL and swing were 140 mV/V and 90 mV/dec for NMOS, and 205 mV/V and 140 mV/dec for PMOS, respectively.

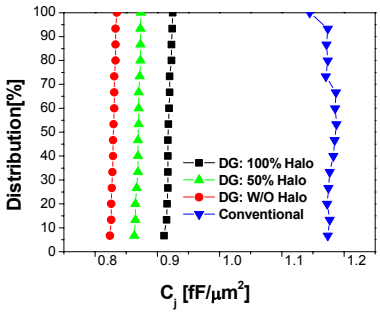

Fig. 8. Comparison of NMOS junction capacitance between damascene gate scheme and conventional scheme. With damascene gate process, C*j* can be reduced by 23 %.

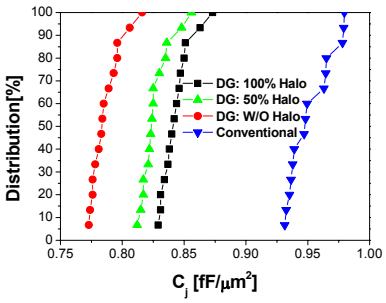

Fig. 9. C*j* comparisons of PMOS between damascene gate scheme and conventional scheme. C*j* can be reduced by 11 %.

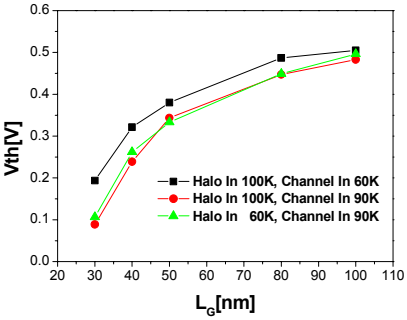

Fig. 10. Vt controllability with vertical junction depth and lateral graded profile.

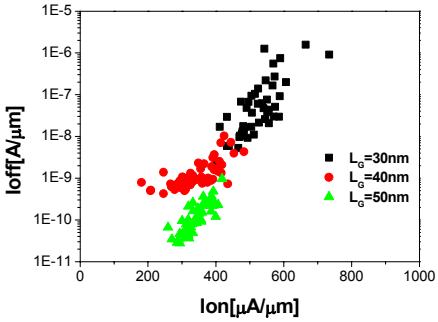

Fig. 11. Ion vs. Ioff characteristics for various Lg. It shows that damascene gate scheme can be highly manufacturable and reliable in sub 30 nm regime.