Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 440-441

P2-19

A Novel High Ruggedness Power MOSFET With a Planar Oxide Deep P+ Implant Structure

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1. Introduction

In past decades, vertical power MOSFETs were widely used in many applications, such as, power supply, DC-DC converter, motor drive and so on. Most of these applications require the MOSFET be switched on and off with an inductive load. Under this condition, the MOSFET must sustain a great deal of stress without causing destructive failure and this ability is called the device "ruggedness". In general, the power MOSFET ruggedness is defined the amount of avalanche energy that can sustain the avalanche current under a single shot unclamped inductive load switching (UIS). Figure 1 illustrates this single shot UIS test circuit.

In order to improve the device ruggedness, many investigations were present in recent years [1-3]. In these studies, the authors use a sacrificial spacer to implant a shallow surface diffused P+ region under the n+ source region to improve the avalanche energy. However, this method need to add an exactly, hard-controlled sidewall process in the original process [4]. In this work, a novel high ruggedness performance power MOSFET has been developed which was using a planar oxide deep p+ implant process. Figure 2 shows the cross section of the proposed device structure.

2. Device Fabrication

We use three different structures to compare the devices ruggedness with each other. Figure 3 (a) shows the conventional heavy p+ body process flow. In this process, the heavy body region is fabricated by using a P+ mask to improve the avalanche characteristics. Figure 3 (b) shows a contact implant process, which can reduce one mask. In this process, the cost of the P+ mask can be saved. However, this process has a drawback owing to no enough anneal time to drive the P+ in after heavy p+ body implant. Therefore, the heavy p+ body region will be small and the avalanche capability will be reduced.

In order to overcome this drawback and reduce the cost of the device fabrication, a novel device fabrication was developed and illustrated in Figure 3 (c). We use a planar oxide layer to replace the spacer process, which is mentioned in [3]. The heavy P+ body region was implanted after depositing a LTO layer. Figure 4 (a), (b) and (c) show the SEM pictures of those devices, respectively. We can observe the heavy p+ body areas are quite different with each other. A wide P+ body area indicates a higher avalanche energy characteristic.

3. Experiment and Result

Figure 5 (a), (b) and (c) show the measured devices avalanche characteristics under the UIS test, respectively. The test condition is V_{DD}=15V, L=94.3 uH, V_G=10 V and R_G=25 Ω. All devices are identical except process. All devices have the same area of 3.24 mm^2. We can see the ruggedness of the LTO process Power MOSFET have great improvement than others.

Table 1 summarizes the measured avalanche current and energy results. It can be found the device avalanche energy with LTO process is improved about 355% than the original process. From the SEM pictures, we can observe the LTO device has a wide heavy P+ body region than the original and contact implant process. This wide heavy body region can reduce the p body sheet resistance and avoid the parasitic bipolar transistor turn on. Besides, the LTO process is another kind of self-aligned process. Therefore, the heavy body can always be formed at the same location in each cell and can avoid the vibration of the avalanche energy, which was caused by the photolithography miss-align of the heavy body implant.

4. Conclusions

A novel high ruggedness performance power MOSFET has been proposed and discussed by using a planar oxide deep p+ implant process. From the UIS test, the avalanche energy can improve about 355% than the conventional process.

References

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[3]Sameer Pendharkar, Malay Trivedi, Krishna Shenai, IEEE Trans. Electron Devices, Vol.45, No.10, 2222 (1998)

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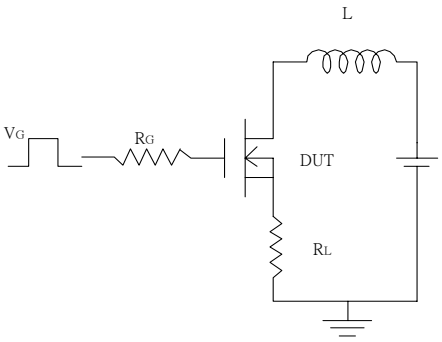


Figure 1 The UIS test circuit

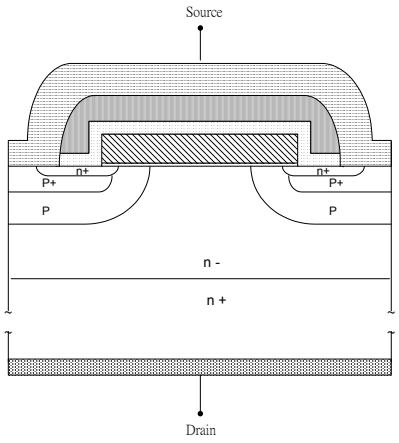
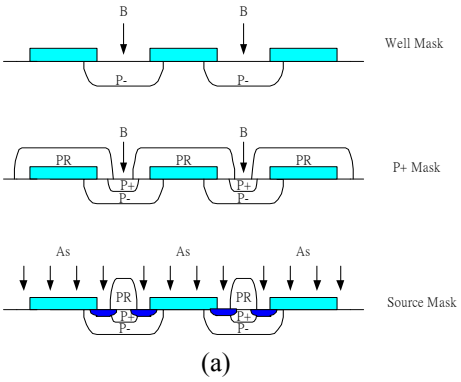
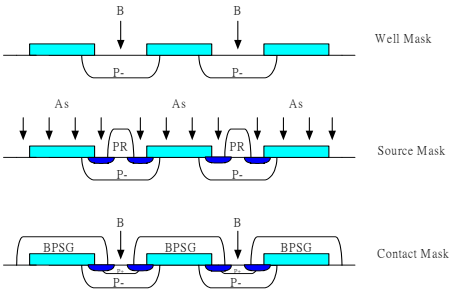


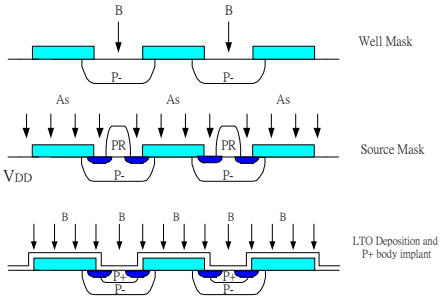
Figure 2 The cross section of Power MOSFET using the LTO process



(a)



(b)



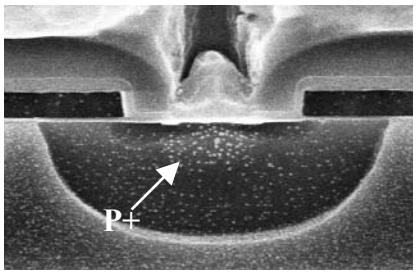
(c)

Figure 3

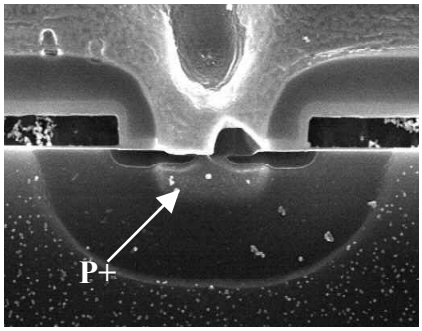
(a) The conventional p+ mask process

(b) The contact p+ implant process

(c) The LTO p+ process



(a)



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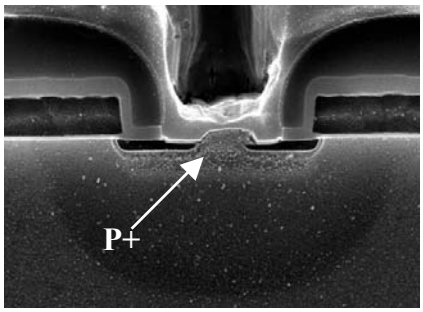


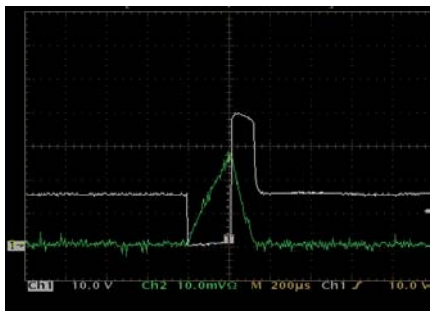
(c)

Figure 4 The device SEMs of

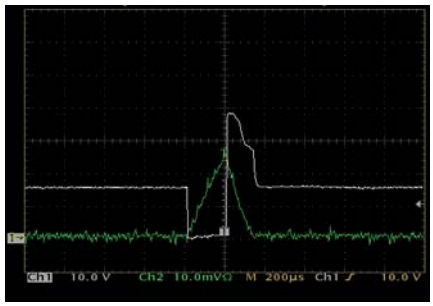
(a) The conventional p+ mask process

(b) The contact p+ implant process

(c) The LTO p+ process



(a)



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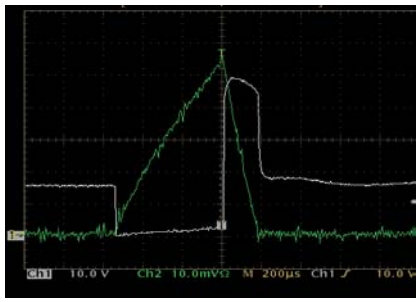

(c)

Figure 5 The UIS waveforms of

(a) The conventional p+ mask process

(b) The contact p+ implant process

(c) The LTO p+ process

Table I The measured avalanche current and energy

	Conventional process	Six mask process	LTO process
Avalanche Current (A)	27.4	24.6	54.6
Avalanche Energy (mJ)	57.1	47.3	203.3