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Novel Nitrogen doped Ni SALICIDE Process for Nano-Scale CMOS Technology

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1. Introduction

Nickel silicide is considered to be the most suitable material for nano-CMOS, self-aligned silicide (salicide) applications. Key advantages of nickel silicide over other silicides include low resistivity, less Si consumption, less line-width sensitivity, lower reaction temperature for silicide formation, and smaller contact resistance [1,2]. However, the main drawback of Nickel Silicide is poor thermal stability, that is, large increase of junction leakage current and sheet resistance degradation by subsequent thermal processes. Multi-structures [3], alloy target of NiTa [4], TiN or Ti capping, heavy ion induced PAI (Pre-Amorphization Implantation) such as As, Ge, or N_2 [5-7] methods have been reported to improve resistance without degradation.

In this paper, novel NiSi technology using the 1%-Nitrogen doped Nickel target has been proposed to nano-scale CMOS technology. The proposed NiSi showed great improvement of thermal stability of sheet resistance and device performances without degradation of junction leakage current.

2. Experimental

For experiment, nano-scale CMOSFETs with a physical gate length of 80 nm is fabricated using a 90 nm CMOS technology. A brief fabrication process flow is shown in Fig.1. After applying normal CMOS processes up to Source/Drain RTP annealing, N-doped Ni and TiN capping (10/25nm) were sputtered sequentially. Then, NiSi was formed by RTP anneal in the temperature range of 400~800℃ (Fig. 1). Then, unreacted metals were selectively removed by wet etching etching (H_2SO_4 : H_2O_2 = 4:1). Finally, post silicidation furnace annealing is applied at 650℃ for 30min in the furnace for evaluation of thermal stability of NiSi. Nickel silicide with pure Ni with TiN capping is also fabricated for comparison. The device performance, sheet resistance according to line width and junction leakage current; areal (W × L = 200 × 250 ㎛) and peripheral (W × L = 0.5 × 250 ㎛, 240 ea) intensive diodes as well as the device parameters were measured by HP4156C semiconductor analyzer. Ni silicide / Si interface uniformity was confirmed by XTEM (Cross-sectional Transmission Electron Microscopy)

3. Results and Discussion

Nickel silicide with the N-doped Ni shows wider temperature window as shown in Fig. 2. Moreover, thermal stability of N-doped silicide shows better thermal stability than pure silicide (Fig. 2(b)). N-doped NiSi also showed stable sheet resistance down to 80 nm gate length in spite of 650 ℃, 30 min annealing as shown in Fig. 3. In case of pure NiSi, sheet resistance was abruptly increased. Fig. 4 shows the TEM image of 80 nm NMOSFET. Nickel silicide is formed uniformly on source/drain and gate-poly regions.

Figure 5 shows the junction leakage current before and after the furnace annealing. In case of pure nickel, junction leakage currents of both areal- and peripheral-intensive diode are increased a lot after furnace annealing. On the other hand, for Nitrogen doped nickel, junction leakage current was decreased after furnace annealing which is believed to be due to the retardation of Ni diffusion by Nitrogen atoms which can stuff in grain boundaries while dopants were diffused a little.

Figure 6 indicates similar V_T dependence of NMOSFET with N-doped NiSi with Pure NiSi on the gate length. The I_D-V_{GS} characteristics of 80nm NMOS shows little degradation of device performance in spite of 650 ℃, 30 min annealing as shown in Fig. 7. Moreover, the proposed method showed a little improvement of device performance, that is, off current, I_{off} decrease about 32% and drive current, $I_{d,sat}$ increase approximately 5% compared with pure-Ni case as summarized in Table 1.

4. Conclusions

Nitrogen doped Nickel was used to improve the thermal stability of Ni-silicide for nano-scale NMOSFETs. Thermal stability of nickel silicide is improved by the Nitrogen incorporation in NiSi layer. Even after the post-silicidation annealing at 650 ℃ for 30min, the low resistivity NiSi with low junction leakage can be achieved. Moreover, improved device characteristics such as trans-conductance, on-off current, subthreshold slope were obtained in physical length of 80nm NMOSFET. Therefore, the proposed method is highly promising for nano-scale CMOS technology.

Acknowledgements

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References

[1] Q. Xiang., Abst.of 201st Electrochem. Soc. Meeting, 583 (2002).
[2] Y. Hu, S. P. Tay, J. Vac. Sci. Tech. (B), 19, 2, 376 (2001).
[3] M. Y. Wang et al., Symp. On VLSI Tech. Dig., 157 (2003).
[4] M. C. Sun et al., Symp. On VLSI Tech. Dig., 81 (2003).
[5] C. T. Huang et al., IEEE Electron Dev. Lett., 17, 3, 88 (1996).
[6] T. Ohguro et al., IEDM 453 (1995).
[7] T. S. Chao et al., JJAP 41, L381 (2002).

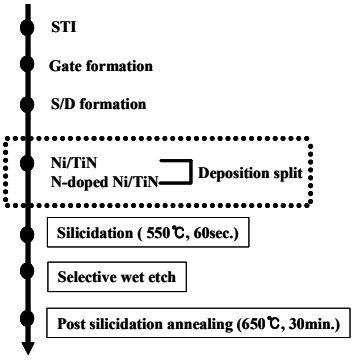
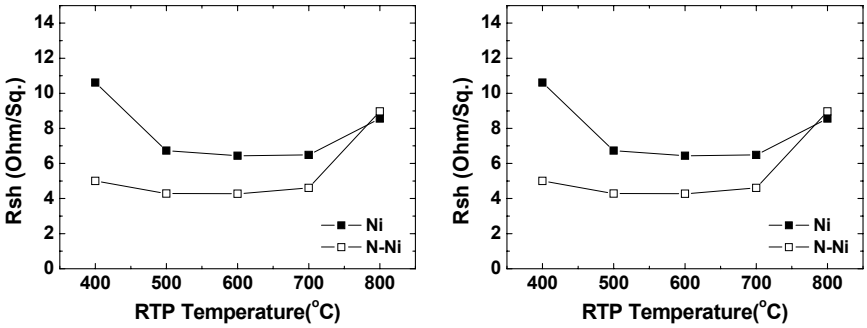
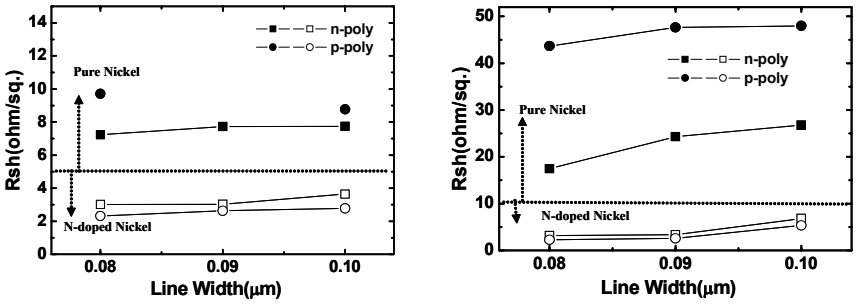


Fig. 1 The key process flow for fabrication of CMOSFETs.



(a) (b)

Fig. 2 Phase transition and annealing property of NiSi. (a) RTP temperature split, (b) annealing temperature



(a) (b)

Fig. 3 Sheet resistance on poly as a function of line width (a) before (b) after the furnace annealing at 650℃, 30 min. (Solid : pure nickel, Open : nitrogen doped nickel)

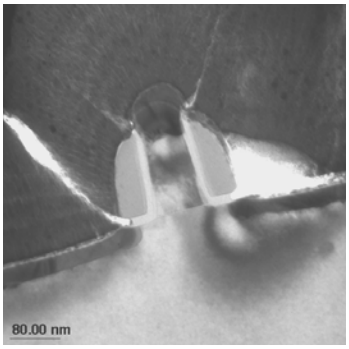
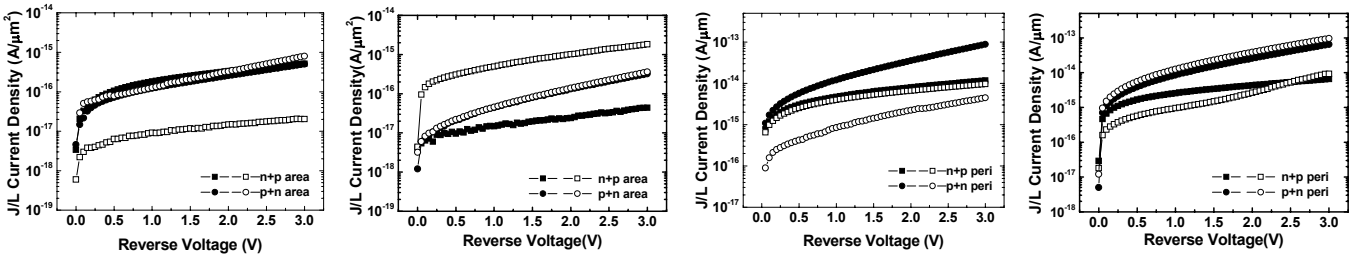


Fig. 4 Cross sectional TEM image of NMOSFET with a gate length of 80 nm.



(a) (b) (c) (d)

Fig. 5 Junction leakage current of (a), (b) area intensive junction (250 m × 200 m) and (c), (d) peripheral intensive junction (250 ×0.5 m ×240). (Solid : without annealing, Open : with annealing.) before and after the furnace annealing at 650℃, 30 min. (a), (c) N-Ni and (b), (d) Ni.

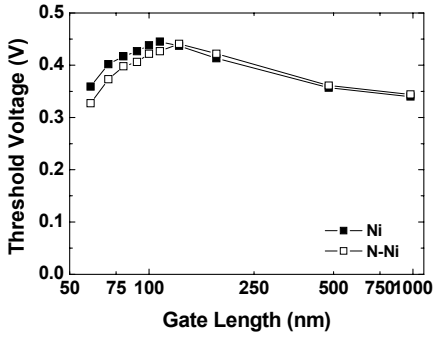


Fig. 6 Threshold voltage roll-off characteristics of fabricated NMOSFETs.

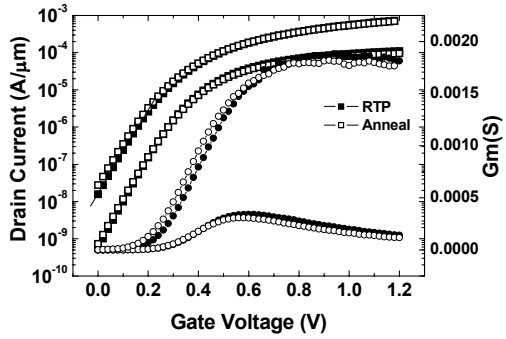


Fig. 7 I_D-V_{GS} characteristics of 80nm NMOS before and after the furnace annealing at 650℃, 30 min.

Table 1. Device performance summary.

parameter	N-Ni	Ni
Lg [nm]	80	80
Id,sat [μA/μm)	680	646
Id,off [nA/μm)	35.2	54
Vth [mV]	327	354
Gm,max [μS]	1480	1348
SS [mV/dec.]	77	85