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Design and Analysis of On-Chip Tapered Transformers for Silicon RFICs

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1. Introduction

Transformers have been the significant circuit components in RF/microwave applications for many decades. Although much research effort has been devoted to this subject and several innovative structures have been presented [1]-[2], the demand for high-performance on-chip transformers is still evident. In this study, we propose the tapered transformer structure, for the first time, based on layout optimization technique [3] to improve the coupling coefficient and quality factor of the RF monolithic transformers. This technique takes into account both the electrically conductive losses and magnetically induced losses of the spiral coils and optimizes the width of the metal strip for each inter-wound winding to enhance the transformer performance. To substantiate our argument, tapered-width transformers and standard equal-width transformer fabricated using the 0.18 µm CMOS process are characterized up to 8.5 GHz with the four-port *S*-parameter measurement system.

2. Experiments

The 0.18 µm 6-level CMOS technology was used to implement the transformers. An 800-nm-thick oxide is deposited on 10-20 Ω·cm p-type silicon substrate. The top metal and the other metal layers are fabricated using 2µm-thick and 0.6µm-thick aluminum alloy, respectively. The thickness of each inter-metal dielectric (IMD) is 1.4 µm. Figure 1 illustrates the top views of the layout of the standard transformer, tapered transformer, and their corresponding dummy structure. Three interleaved spiral transformers with the dimensions of number of turns (N) = 3, turns ratio = 1:1, coil-to-coil spacing (S) = 2 µm, outer diameter (OD) = 400 µm, and different metal widths (W) listed below were designed and fabricated

T1: W_1 = 20 µm, W_2 = 20 µm, W_3 = 20 µm
T2: W_1 = 20 µm, W_2 = 15 µm, W_3 = 10 µm
T3: W_1 = 20 µm, W_2 = 10 µm, W_3 = 2 µm

where W_n is the width of the nth turn of the coil.

Four-port *S*-parameters were measured from 50MHz to 8.5 GHz with an Agilent E5071B RF Network Analyzer and Cascade Microtech HPC probes. Before *S*-parameter measurements, the measurement system was calibrated using the four-port Short-Open-Load-Through (SOLT) calibration method with a calibration substrate.

3. Results and Discussion

After de-embedding the parasitic effects of probe pads, the intrinsic four-port *Y*-parameters of the transformers $[Y^D]$ can be expressed as $[Y^D] = [Y^T] - [Y^O]$, where $[Y^T]$ and $[Y^O]$ are the *Y*-parameters of the transformer and the "OPEN" dummy, respectively. As depicted in Fig. 1, port 2 and port 3 are open-circuited and the intrinsic series resistance (R), self-inductance (L), and quality factor (Q) of the transformers can be calculated from the two-port *Y*-parameters

$$R = \mathrm{Re}\left(\frac{1}{Y_{11}}\right) \tag{1}$$

$$L = \frac{1}{\omega}\mathrm{Im}\left(\frac{1}{Y_{11}}\right) \tag{2}$$

$$Q = \frac{-\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{3}$$

where ω is the angular frequency. By grounding port 3 and port 4, the mutual inductance (M) between the primary and secondary windings and the coupling coefficient (k) are calculated from the two-port *Z*-parameters [4]

$$M = \frac{1}{\omega}\mathrm{Im}(Z_{21}) \tag{4}$$

$$k = \frac{M}{\sqrt{L_{11}L_{22}}} \tag{5}$$

where L_{11} and L_{22} are the imaginary parts of Z_{11} and Z_{22} divided by ω, respectively. Figure 2 shows that the series resistance increases as the widths of the inner windings decrease owing to the contributions of ohmic losses and magnetically induced losses. Figure 3 exhibits that the self-inductance increases as the widths of the inner windings decrease due to the increasing of magnetic flux linkage. As shown in Fig. 4, the transformer *T2* with tapered metal width shows a maximum Q value of 6.9 at 2.4 GHz. According to the above results, we conclude that quality factor of the transformer can be maximized by optimizing the metal width. Figures 5 and 6 display the measurement results of mutual inductance and coupling coefficient, respectively. Results indicate that both the mutual inductance and coupling coefficient increase as the widths of the inner windings decrease due to the rising of magnetic coupling. Figure 7 compares the insertion losses ($|S_{21}|$) of the transformers. At low-frequency regime, the coupling from primary to secondary windings is negligible. As the operation frequency increases, the coupling increases and reaches a maximum in the 2-4 GHz range for these transformers. It is seen that the transformer *T2* shows a maximum $|S_{21}|$ value of –3.7 dB at 3 GHz.

4. Conclusions

A new transformer structure has been proposed and compared with the conventional structure. The proposed structure is symmetric and more area efficient. With the layout optimization technique, the tapered spiral windings can be designed to improve the quality factor, coupling coefficient, and insertion loss of the on-chip transformers.

Acknowledgements

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References

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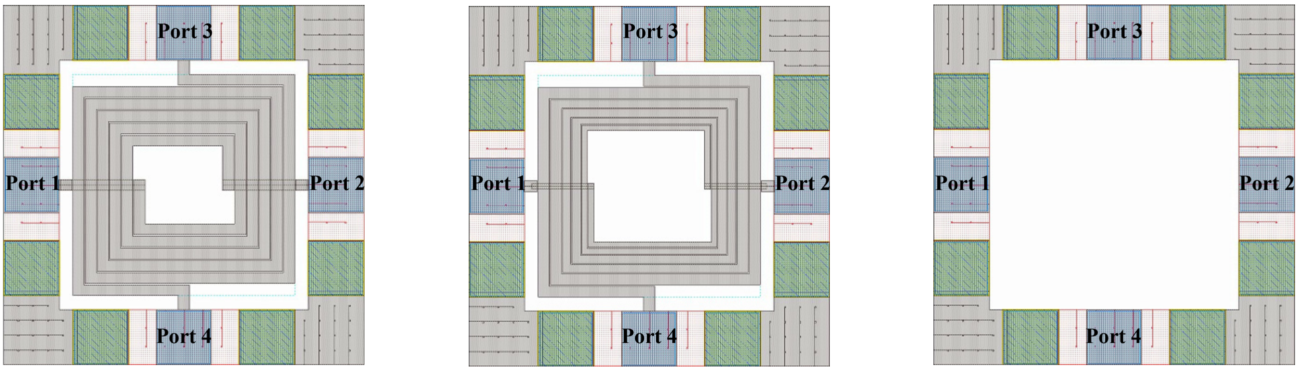

(a) (b) (c)

Fig. 1 Illustration of the four-port 1:1 interleaved transformers. (a) Conventional structure. (b) Proposed structure. (c) Dummy device.

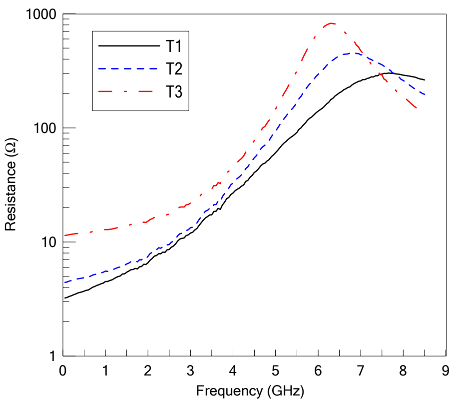

Fig. 2 Effective series resistance for the standard and tapered transformers.

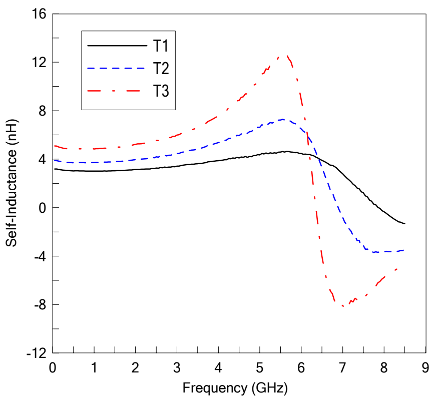

Fig. 3 Self-inductance for the standard and tapered transformers.

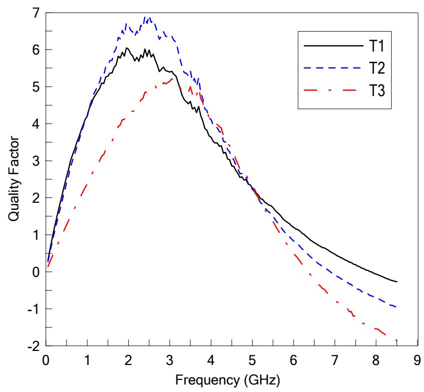

Fig. 4 Quality factor for the standard and tapered transformers.

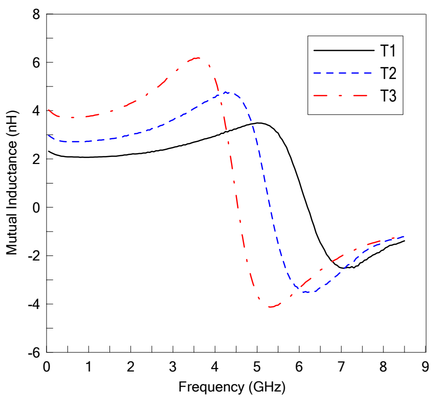

Fig. 5 Mutual inductance for the standard and tapered transformers.

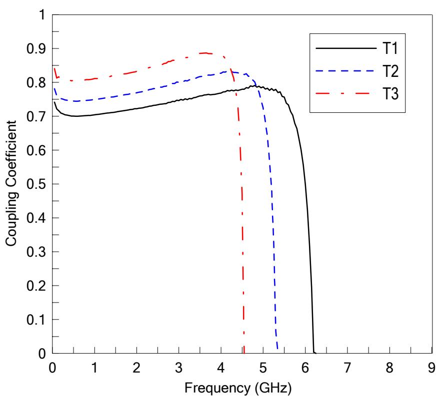

Fig. 6 Coupling coefficient for the standard and tapered transformers.

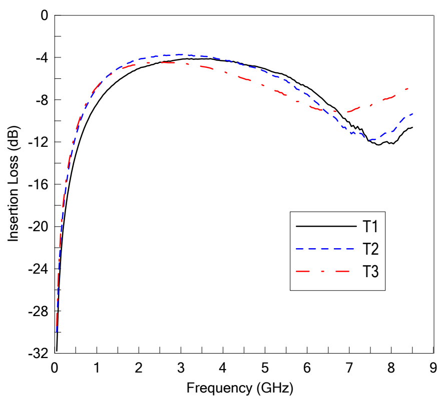

Fig. 7 Insertion loss for the standard and tapered transformers.