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Anomalous Behaviors of Random Telegraph Signals in Ultra-thin Gate Oxide MOSFETs

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1. Introduction

It has been widely recognized [1]-[6] that at room temperature of operation, the relative magnitude ΔI/I of random telegraph signals (RTSs) in drain-to-source current of MOSFETs is nearly constant whereas a roll-off in ΔI/I occurs as gate voltage exceeds the threshold voltage. On the other hand, the RTS magnitude ΔI itself has been relatively less studied.

In this paper, we present for the first time anomalous behaviors of ΔI/I, exactly opposed to the literature [1]-[6]. The origin of such difference is due to ultra-thin gate oxide used in this work, which in turn gives rise to significant quantum confinement effect. To confirm this hypothesis, a self-consistent Schroedinger-Poisson solver is performed. In addition, the underlying ΔI also for the first time exhibits another anomalous behaviors and is addressed in the similar way.

2. Experimental and Results

The 1.7-nm gate oxide n-channel MOSFETs with two aspect ratios of W/L = 130 nm/80 nm and 100 nm/170 nm were fabricated. The corresponding threshold voltage was 0.22 V and 0.28 V, respectively. The devices biased in linear condition (V_D = 10 mV) were characterized at room temperature, employing a special technique [7] to find the possible RTS events. Only with the presence of a potential trap can such discrete switching be observed. We found that the same fluctuations simultaneously occur in both source and drain current, as shown in Fig. 1. The trap responsible is likely the process-induced defect. No noticeable fluctuations in the gate or bulk current were observed. The RTS recorded as function of gate voltage is depicted in Fig. 2.

Two new observations were produced for the first time. The first is the anomalous dependence of ΔI/I on gate voltage as displayed in Fig. 3: ΔI/I dramatically increases as gate voltage is decreased from above-threshold through the threshold point to the weak inversion region. This is exactly opposed to the arguments made in the literature [1]-[6]. *Such difference apparently reflects the fact that the gate oxide thickness used in [1]-[6] was much larger than ours.* In other words, only with ultra-thin gate oxide scale (i.e., 1.7 nm in this work) can the quantum confinement effect be profound. The second new observation is that the magnitude ΔI versus gate voltage as given in Fig. 4 looks like a bell shape, which again is not reported elsewhere.

3. Analysis and Discussion

The contribution of channel carrier number fluctuations to RTS in drain-to-source current can be described by [8]

$$\frac{\Delta I}{I} = \frac{\alpha q C_{inv}}{W_{eff} L_{eff} Q_{inv} (C_{eff} + C_{inv} + C_{dep})} \qquad (1)$$

C_{inv} and C_{dep} are the capacitance per unit area of 2DEG (2-dimensional electron gas) inversion layer and bulk depletion region, respectively. The effective capacitance C_{eff} is equal to $C_{ox}C_{poly}/(C_{ox}+C_{poly})$ where C_{ox} and C_{poly} are the capacitance per unit area of gate oxide and polysilicon depletion, respectively. L_{eff} and W_{eff} are the channel length and channel width, respectively. Q_{inv} is the inversion-layer charge per unit area, and α is the screening coefficient.

As explained in the preceding section, quantum treatment of the issue is essential. To achieve this goal, fitting of experimental gate oxide C-V was first carried out using a self-consistent Schroedinger-Poisson solver, leading to values of process parameters. Then the same Schroedinger-Poisson solver straightforwardly furnished the detailed information as plotted in Fig. 5 and 6. Substituting these quantities into (1) yields the ΔI/I as shown in Fig. 7. It is thereby argued that the observed anomalous behaviors are due to quantum confinement effect. The noticeable deviations from the data might be ascribed to mobility fluctuations (or Coulombic scattering) and/or uncertainties in L_{eff} or W_{eff} determination.

Finally, to facilitate the analysis, the drain-to-source current is written as $I = W_{eff}Q_{inv}\upsilon_{eff}$, where υ_{eff} is the effective carrier velocity implicitly including the mobility. Substituting this into (1), we obtain

$$\Delta I = \frac{\alpha q C_{inv} \upsilon_{eff}}{L_{eff} (C_{eff} + C_{inv} + C_{dep})} \qquad (2)$$

The measured source current is given in Fig. 8 and since Q_{inv} is known the υ_{eff} can be readily extracted as plotted in Fig. 9. Then the ΔI is calculated using (2) with α = 1 [8]. The results are plotted in Fig. 10 along with experimental data. Strikingly, the bell shape is reasonably described. Better improvements in above-threshold can be achieved with α = 0.5 [8]. The remaining deviations can be attributed to the other mechanisms mentioned above.

4. Conclusion

Two anomalous behaviors concerning RTS magnitudes have been observed. Experimental observations have been reasonably interpreted using a quantum simulator.

Acknowledgement

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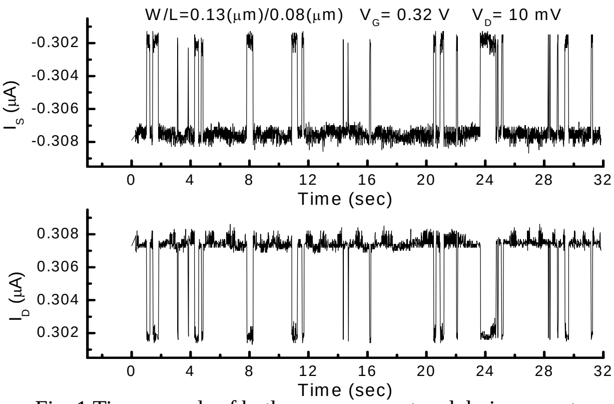

Fig. 1 Time records of both source current and drain current.

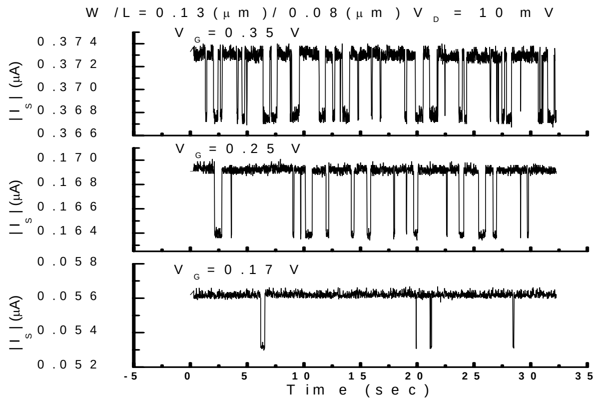

Fig. 2 RTS recorded as function of gate voltage.

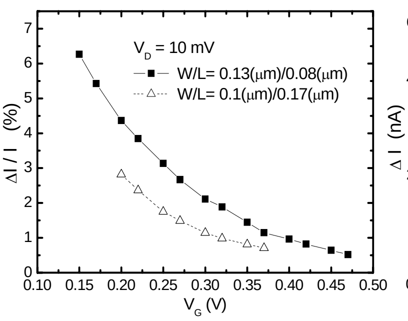

Fig. 3 Measured ΔI/I versus gate voltage.

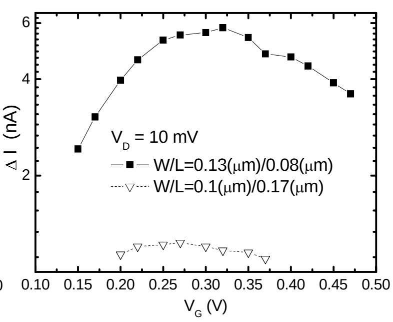

Fig. 4 Measured ΔI versus gate voltage.

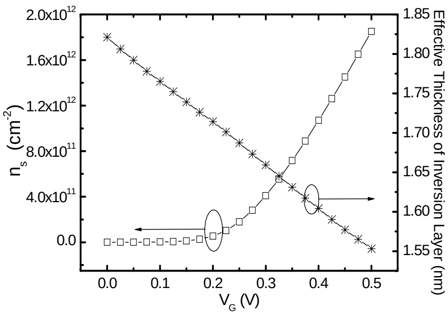

Fig. 5 Simulated carrier density and effective thickness of inversion layer versus gate voltage.

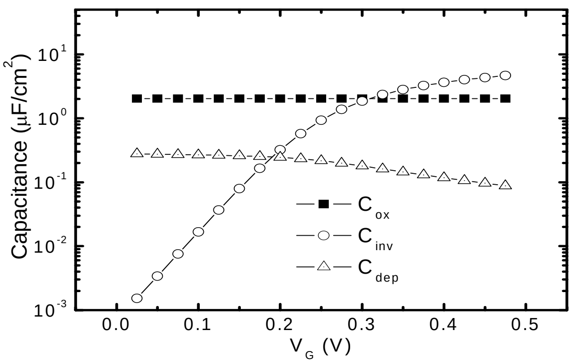

Fig. 6 Simulated capacitances versus gate voltage.

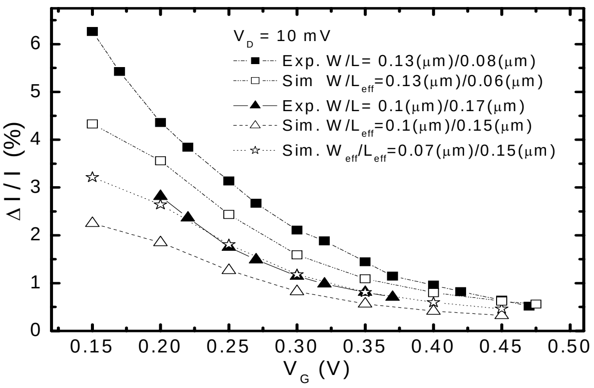

Fig. 7 Simulated and experimental ΔI/I as function of gate voltage.

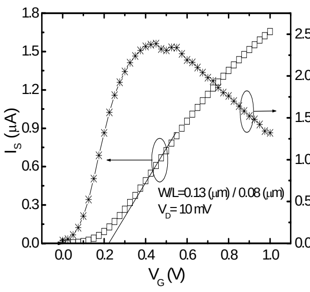

Fig. 8 Measured source current and transconductance versus gate voltage.

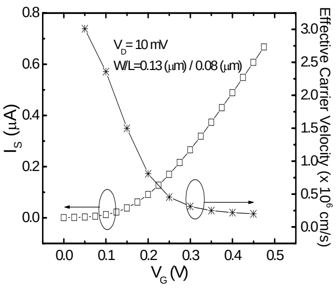

Fig. 9 Extracted effective carrier velocity versus gate voltage.

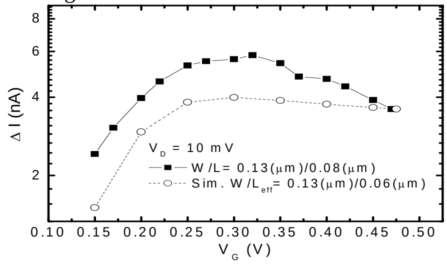

Fig. 10 Simulated and experimental ΔI versus gate voltage.