Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 410-411

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Understanding the Impact of Process Variations on Analog Circuit Performance with Halo Channel Doped Deep Sub-Micron CMOS Technologies

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1. Introduction

Single Halo (SH) and Double Halo (DH) MOSFETs are reported to suppress short channel effects in the sub 100nm regime [1]-[2]. Also, it has recently been shown that SH technologies exhibit good analog performance (higher output resistance and intrinsic MOSFET gain), even down to the sub 100 nm gate length regime [3]-[4]. However, the sensitivity of device and circuit performance parameters on the process variations still needs to be systematically investigated for all these technologies. In this work we present the effect of process variations on analog circuit performance parameters and the impact of halo doping on the circuit linearity with these technologies. Extensive 2-D process, device and mixed mode simulations have been performed to understand this aspect.

2. Simulation Structures

All the simulations have been carried out using ISE TCAD [5]. DIOS process simulator was used for simulating the device structure and DESSIS tool employing the energy balance models was used for device simulations. For the SH and DH MOSFETs used in simulations, V_t is adjusted with a tilt angle implantation after gate patterning. Standard V_t adjustment implant is used for the CON devices. The devices are scaled according to SIA analog roadmap shown in table 1. Unless otherwise specified, the device width is taken as 1μm for simulations.

3. Results and Discussion

Fig. 1 shows the I_D-V_D characteristics of all the three devices with a gate length of 0.1μm at a gate overdrive voltage (V_{GT}) of 0.4 V. The characteristics show that SH MOSFETs result in significant improvement in the output resistance (R_o) and drive currents due to a suppression of the short channel effects. As can be seen, the performance of DH devices lies in between CON and SH MOSFETs. Fig. 2 shows the threshold voltage sensitivity to V_t implant dose (D), oxide thickness (t_{ox}) and channel length (L), arising from the process variations. Except for channel length variations, SH devices exhibit a higher sensitivity to process parameter variations as compared to the CON MOSFETs. Fig. 3 shows the normalized low frequency gain of the three CS amplifiers as a function of V_t variation at a bias current of 0.1 mA. The percentage change in voltage gain as a function of peak input signal voltage is also plotted in the same, estimate the circuit linearity, with the DC gain for all the technologies adjusted to be identical. One can notice that the circuits with SH devices exhibit higher tolerance to V_t variation in addition to an improved linearity. This can be attributed to their well-controlled short channel effects. Fig 4 shows the normalized gain of a source follower circuit as a function of V_t variation along with the percentage change in the gain, as a function of peak input signal voltage. It can be noticed that SH source follower circuits are less sensitive compared to the DH technologies. However, an enhanced body effect in these halo MOSFETs degrades the non-linearity to some extent.

Fig 5(a) shows the percentage change in current transfer ratio (I_{out}/I_{in}) of a current mirror circuit as a function of V_t mismatch. It can be noticed that, for the SH devices, the deviation of the current transfer ratio from its ideal value is minimized. Fig. 5(b) shows the normalized CMRR value for a differential amplifier as a function of V_t mismatch for the worst-case condition ($V_{tM1}= V_{t0}+\Delta V_t/2$, $V_{tM2}=V_{t0}-\Delta V_t/2$, V_{t0} being the actual threshold voltage) for all the three technologies. The transistor sizes for all the three amplifiers and its performance indices are shown in Table 2. One can also notice that the change in CMRR with V_t mismatch is suppressed for the case of SH devices, when compared with the CON devices. Fig 6(a) shows the charge injection error in a simple Sample-and-Hold (S/H) circuit with all the three technologies. The input signal applied is a 0.1 V peak sinusoidal voltage with a 0.5V offset. The reduced error voltage with SH devices is because of the reduced inversion charge present at the source side, due to the high pocket doping present in this region. Fig 6(b) shows the normalized error voltage as a function of V_t variation. There is not much significant change in these values with halo MOSFETs. However, it can be noticed from Fig 6(c) that the large-signal non-linearity is more apparent for halo devices due to the higher body effect

4. Conclusions

Though SH and DH MOSFETs show a higher sensitivity to the process variations, their improved short channel performance reduces this effect at the circuit level. As shown with different analog circuit simulations, the results indicate that about 25% higher V_t mismatch is tolerable with the SH technologies when compared to CON technologies. Our work also shows that improved current saturation in output characteristics of SH MOSFETs translates into a reduced non-linearity for analog circuits. However, enhanced body effect in these devices offsets this advantage to some extent. Our simulations also confirm that halo devices result in reduced charge injection errors in S/H circuits.

5. References

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[3]. H.V. Deshpande, B. Cheng and J.C.S. Woo., *IEEE Electron Dev. Lett.*, (2001), 588.
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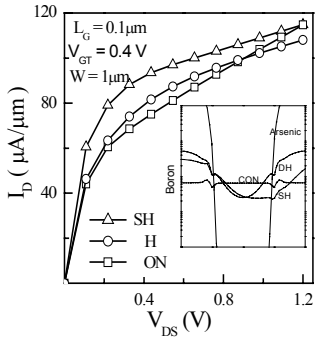

Fig. 1 I_D-V_D characteristics of all devices, Inset: Doping along the channel

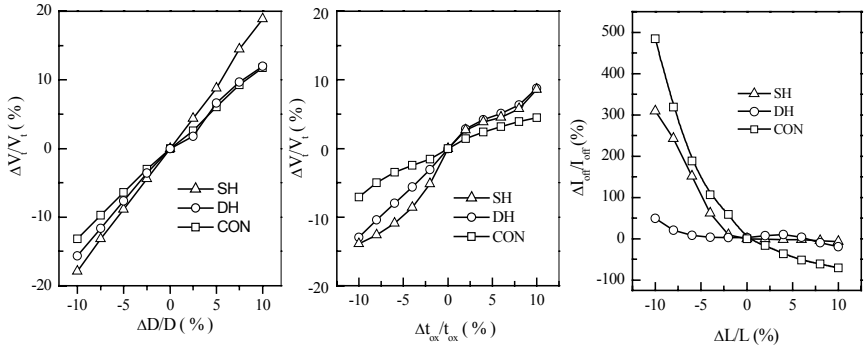

Fig. 2 Threshold voltage sensitivity to dose and oxide thickness, leakage current sensitivity to channel length for CON, DH and SH devices

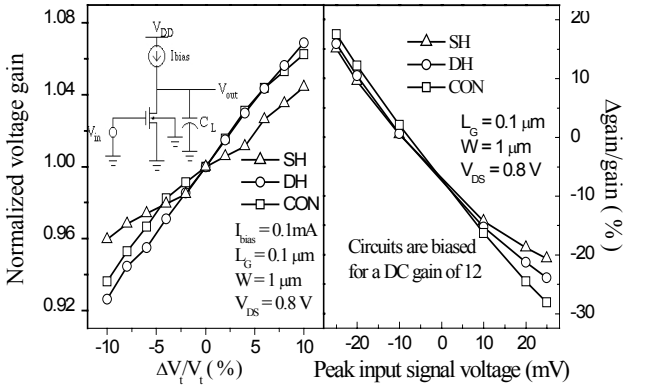

Fig. 3 Normalized voltage gain of CS amplifier as a function of threshold voltage variation and percentage change in gain of the same circuit as a function of peak input voltage for all technologies.

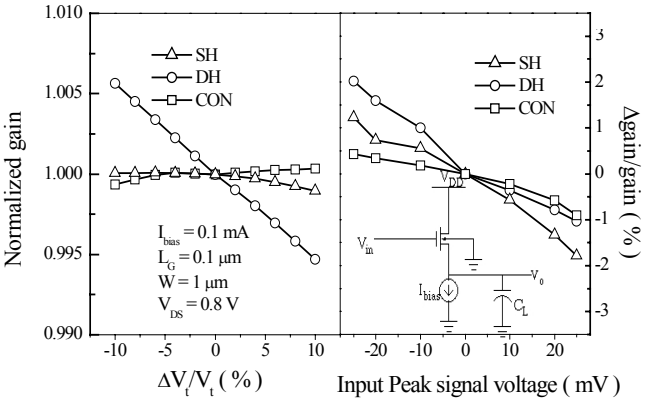

Fig. 4 Normalized voltage gain of source follower as a function of threshold voltage variation and percentage change in gain of the same circuit as a function of peak input voltage for all technologies.

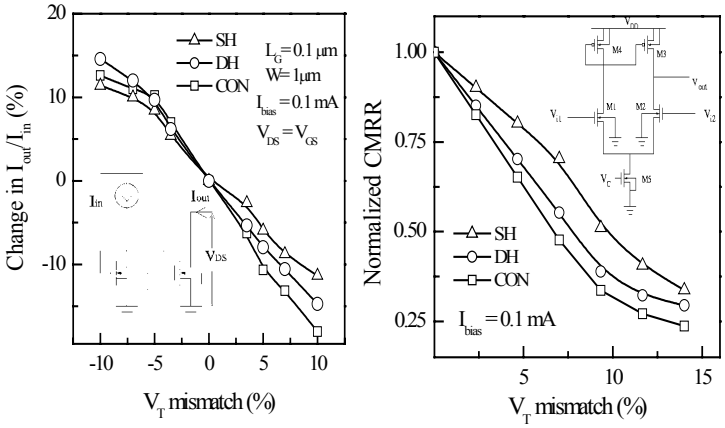

Fig. 5(a) Percentage change in I_{out}/I_{in} versus percentage V_t mis-match, (b) Normalized CMRR versus V_t mismatch for differential amplifiers realized with SH, DH, and CON technologies.

L_G	100 nm
t_{ox}	3 nm
V_t	0.3 V
X_j	30 nm
S/D depth	65nm

Table 1. Process parameters for 0.1μm device

	LAC	DH	CON
W/L u/u (M1M2)	0.48/0.1	0.4/0.1	0.5/0.1
W/L u/u (M3M4)	1.5/0.25	2.1/0.25	2.623/0.25
W/L u/u (M5)	2.85/0.25	3.65/0.25	3.85/0.25
P_d mW	0.2	0.2	0.2
A_V	28.202	10.727	12.803
CMRR dB	60.60	50.21	54.3

Table 2. The transistor sizes required for differential amplifier with V_{DD}=2V and its performance, LAC refers to SH

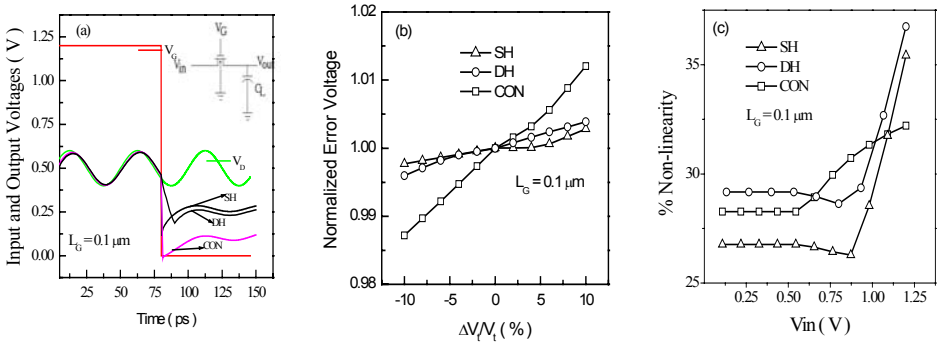

Fig. 6(a) A transient sinusoidal response of the basic S/H circuit to describe the charge injection errors with CON, DH and SH technologies, (b) Normalized error voltage as a function of threshold voltage variation, and (c) Percentage non-linearity of the circuit as a function of input large signal voltage.