

Improvements of Electrical Properties with Reduced Transient-Enhanced-Diffusion for 65nm-node CMOS Technology using Flash Lamp Annealing

Akira Mineji, Koji Yamashita, Fumio Ootsuka, Mitsuo Yasuhira and Tsunetoshi Arikado

Research Dept. 1, Semiconductor Leading Edge Technologies, Inc.
16-1 Onogawa, Tsukuba, Ibaraki, 305-8569, Japan
Phone: +81-29-849-1293 E-mail: mineji@selete.co.jp

1. Introduction

For the 65nm CMOS node technology, especially for sub-50nm gate device fabrication, not only improvement of short channel effect(SCE) but also high drive current must be achieved. Conventional implantation and spike annealing approaches cannot easily realize the junction consistent with the ITRS requirements. One of the problems of ion implantation process is the transient-enhanced-diffusion (TED) caused by point defects [1]. Point defects such as interstitial-Si induced by implantation damage enhance impurity diffusion during the following activation annealing [2]. The redistribution at source/drain and channel dopant caused by TED deteriorates device characteristics such as threshold voltage control, effective channel length or lateral diffusion length modulation (Fig. 1). It has been reported that flash lamp annealing (FLA) technique realizes lower sheet resistance, shallower junction depth and less crystal defects [3, 4]. However, FLA process has currently unsolved integration problems.

This paper presents that 50nm gate CMOS devices can be fabricated by conventional spike annealing process and additional FLA technique without degrading electrical characteristics. The influence of TED reduction by FLA was evaluated from electrical properties.

2. Experimental

CMOS devices were fabricated using the standard process with SiON gate insulator and pre-doped poly-Si electrodes. After the offset sidewall spacer formation, source and drain region was fabricated as shown in Fig. 2. Boron halo implants was used for NMOS and arsenic halo implants was used for PMOS. Low energy implantation of As and B was performed for source and drain extension (SDE) for NMOS and PMOS, respectively. FLA was applied for the purpose of the reduction of point defects induced by halo and SDE implantation damage. After the sidewall formation, the source and drain implantation was performed with As and BF₂. The activation of S/D dopants was carried out by spike annealing at 1050°C with or without FLA prior to the annealing.

3. Results and Discussion

Fig. 3 shows V_{th} roll-off characteristics of PMOS with FLA(Ext-FLA) or spike RTA(Ext-RTA) prior to sidewall formation. The threshold voltage (V_{th}) at long channel devices can be lowered without SCE degradation due to the reduction of halo redistribution to the channel. Ext-FLA process improves pFET's drive current by 7% as

compared with conventional process as shown in Fig. 4. On the other hand, the drive current degraded for the case of Ext-RTA at 900°C. Fig. 5 shows C-V characteristics of PMOS, which indicates that the inversion capacitance is the same. From these results, the drive current reduction for the case of Ext-RTA may be caused by the increased sheet resistance of SDE due to the out diffusion from Si substrate surface or inactivation during Ext-RTA.

Impact of the TED reduction process on nFET's V_{th} roll-off characteristics is shown in Fig. 6. nFET's V_{th} roll-off can be improved by using Ext-FLA process as compared with conventional process. Furthermore, further improvement of the SCE was observed by adding FLA (SD-FLA) prior to S/D spike RTA. Fig. 7 shows NMOS I_{on}-I_{off} characteristics. The Ext-FLA process improves the drive current by 2% and further adding SD-FLA improves the drive current by 4%. N+/p junction leakage measurements in Fig. 8 implies that the S/D junction abruptness was improved by the reduction of TED. Figs. 9 and 10 show V_{th} roll-off and I_{on}-I_{off} for pFETs, respectively. The effect of SD-FLA was very small. Cumulative probability of p+/n junction leakage current is shown in Fig. 11. Similar junction leakage between with and without SD-FLA process indicates that the S/D junction abruptness was the same. For PMOSFETs in this work, the influence of TED was not dominated by the deep source and drain implantation, but by the halo and extension implantation.

From these results, FLA prior to spike RTA process is effective to minimize TED and to prevents the redistribution of the halo and source/drain dopants.

4. Conclusion

The improvements of SCE and the drive current enhancement for 65 nm-node CMOS devices was achieved by conventional spike anneal process and additional FLA. This indicates that halo, SDE and S/D implantation damage can be reduced by FLA without degrading electrical characteristics.

References

- [1] D. J. Eaglesham, et al., Appl. Phys. Lett 65 p. 2305 (1994)
- [2] S. Shishiguchi, et al., VLSI Tech. Symp., p. 134 (1998)
- [3] T. Ito, et al., Ext. Abst IWJT, p. 23 (2002)
- [4] K. Yamashita, et al., Ext. Abst SSDM, p. 742 (2003)

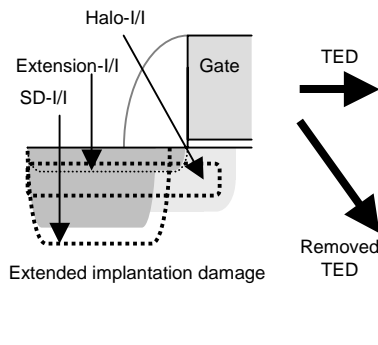
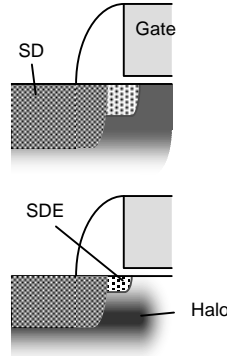


Fig. 1 Schematic illustration of the source/drain structure with halo and SDE, and effects of TED on SD and channel regions.



- ◆ Halo I/I
- ◆ Source/Drain Extension I/I
- ◆ **FLA or Spike-RTA**
- ◆ Sidewall Formation
- ◆ Source/Drain I/I
- ◆ **FLA (SD-FLA)**
- ◆ Spike-RTA
- ◆ Ni salicide process

Fig. 2 Process step for fabrication of the CMOS devices.

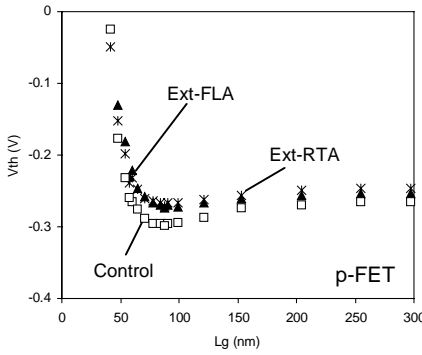


Fig. 3 V_{th} Roll-off characteristics for PMOS without SD-FLA.

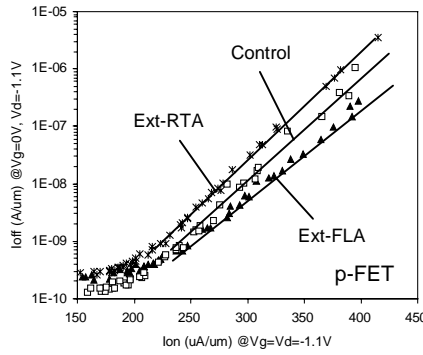


Fig. 4 I_{on} - I_{off} characteristics for PMOS without SD-FLA.

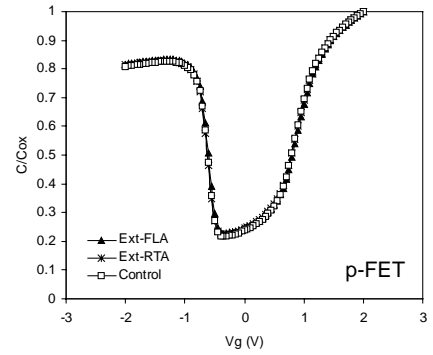


Fig. 5 C-V characteristics for PMOS without SD-FLA.

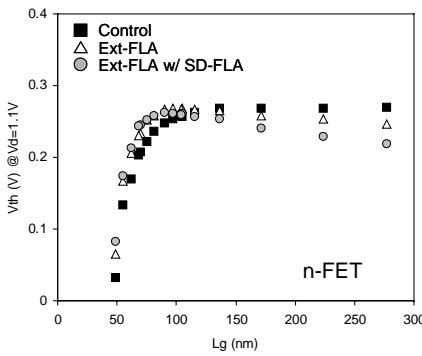


Fig. 6 V_{th} Roll-off characteristics for NMOS with Ext-FLA and with or without SD-FLA.

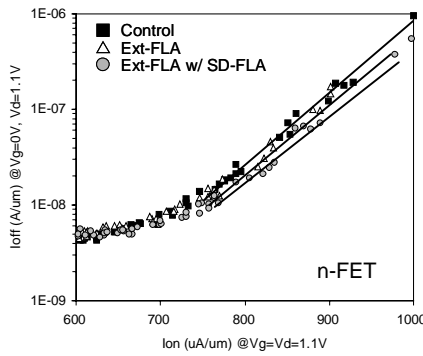


Fig. 7 I_{on} - I_{off} characteristics for NMOS with Ext-FLA and with or without SD-FLA.

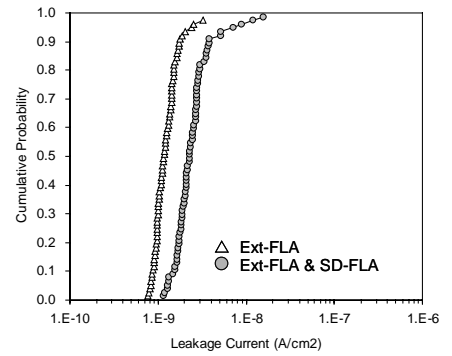


Fig. 8 Cumulative probability of n+/p junction leakage current with Ext-FLA and with or without SD-FLA.

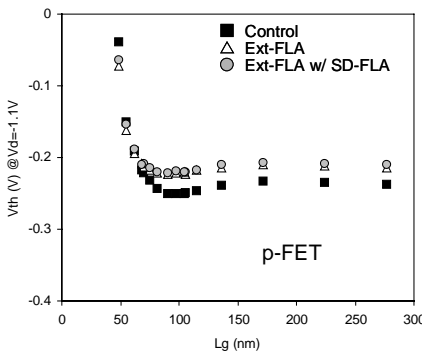


Fig. 9 V_{th} Roll-off characteristics for PMOS with Ext-FLA and with or without SD-FLA.

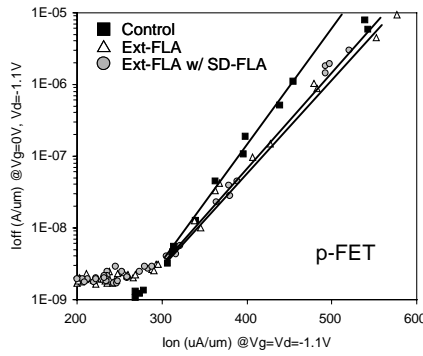


Fig. 10 I_{on} - I_{off} characteristics for PMOS with Ext-FLA and with or without SD-FLA.

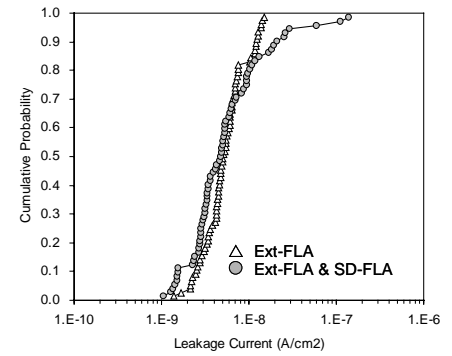


Fig. 11 Cumulative probability of p+/n junction leakage current with Ext-FLA and with or without SD-FLA.