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Strain Dependence of Mobility Enhancement in Local Strain Channel nMOSFETs

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1. Introduction

As the scaling of CMOS structure reaches its fundamental limits, the improvement of carrier mobility has been intensively studied by introducing strain in the channel region, such as strained Si on SiGe substrate [1]. However, the fabrication of the strained Si devices is more complicated, such as forming a relaxed SiGe buffer layer. Recent studies have shown that the uniaxial strained channel from a contact etch-stop silicon nitride (SiN) layer affects the current drivability [2]. Unfortunately, uniaxial tensile strain only improves the electron mobility but degrades the hole mobility and the compressive strain is in the opposite direction. In order not to degrade either of them, Local Mechanical-Stress Control (LMC) technique has been demonstrated [3]. It utilized a SiN capping layer with high mechanical stress and selective Ge-ion implantation into the SiN layer, can improve the performance of nMOSFETs and pMOSFETs simultaneously. However, additional Ge implantation process has to increase one more photo alignment in CMOS process. For this reason, the local strained channel (LSC) technique is proposed which provides tensilely strained channel only in nMOSFETs by forming compressively strained poly silicon (poly-Si) gate electrodes [4]. In this study, we proposed a local strained channel technique that using deposition of SiN layer with high mechanical stress on a stacked amorphous silicon (*a*-Si) and poly-Si gate. It was found that the stack of *a*-Si and poly-Si gate could increase tensile strain in the channel region compared to that of the single-poly-Si gate structure.

2. Experiments

The local strain structure with the stack of *a*-Si and SiN capping layer has been fabricated. After RCA cleaning process, 2.5nm gate oxide was grown in a vertical furnace (800°C, O_2 ambient). Then, *a*-Si (550°C, 20-70 nm) and in-situ n^+ doped poly-Si (550°C) were deposited in the same ambient. The final poly-gate thickness was kept the same for all samples. After S/D formation, thermal CVD SiN (780°C,) with different thickness, 20-280 nm, was directly deposited on the transistor and followed by TEOS deposition. After contact alignment, TEOS- and SiN-etch were carried out in the same system. In order to protect the Si surface without etching damage, SiN layer was etched in two-step. We calculated the SiN etch rate and left 20nm after dry etching. Then, we used the H_3PO_4 solution to etch the residual SiN layer. After these processes, (Ti / TiN / Al / TiN) four-level metallization were carried out in PVD system for contact.

3. Results and Discussion

Figure 1 shows the dependence of output characteristics by capping SiN-layer of different thicknesses. The drain current of nMOSFETs with 280 nm SiN layer shows 15% increase compared to that of conventional devices. The transconductance increases with the increase of thickness of SiN-layer as shown in Fig. 2. This result implies that the increase of electron mobility is the cause of the observed enhancement of the drain current. Fig. 3 illustrates the measured C-V profile with different thickness of SiN-layer. The inversion capacitance and flat band voltage are almost the same as that of conventional device. The dependence of threshold voltage on different thickness of SiN-layer is shown in Fig. 4. The results show that the threshold voltage decreases as the thickness of SiN-layer is increased.

The strain effect of the stack of *a*-Si and poly-Si gate was shown in Fig.5. All samples are capped a 50nm SiN- layer for comparison. The drain current is improved 19% for 70nm *a*-Si sample compared to that of the stack with 20nm one. The transconductance increases as the thickness of *a*-Si layer is increased, as shown in Fig.6. The mechanism of the stress elevation could be as follows: before the dopant activation process, the entire n^+-poly gate is in amorphous phase due to the stack of *a*-Si and high dose implantation of arsenic. The re-crystallization of amorphous region during rapid thermal annealing leads to n^+-poly gate expansion, and resulting in residual compressive stress. This compressive stress in n^+-poly gate provides highly tensile strain to the channel region. The threshold voltage is in proportion to thickness of the *a*-Si layer as shown in Fig. 7. This means the strain effect causes the improvement of electron mobility is larger than the effect of increased the threshold voltage. The pronounced increase of transconductance on stack of 50nm *a*-Si layer and different thickness of SiN-layer is shown in Fig. 8. We found that the strain dependence of mobility enhancement is significantly enhanced by using both SiN-layer and stack *a*-Si gate structures.

In summary, we found that a local strain channel to improve the mobility of nMOSFET can be achieved by using a stack-gate poly-Si and capping with a SiN-layer.

Reference

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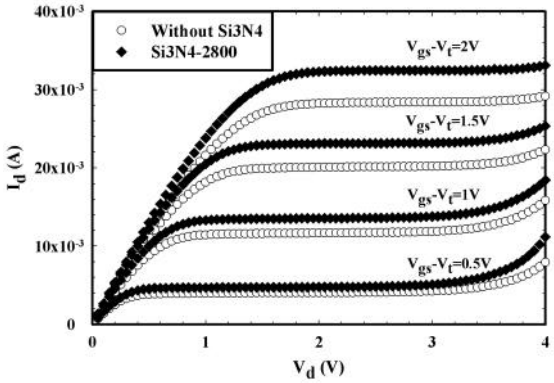

Fig. 1 Output characteristics for different thickness of SiN capping layer.

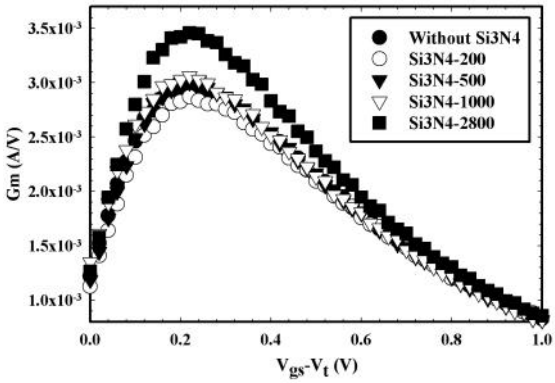

Fig. 2 Transconductance for different thickness of SiN capping layer.

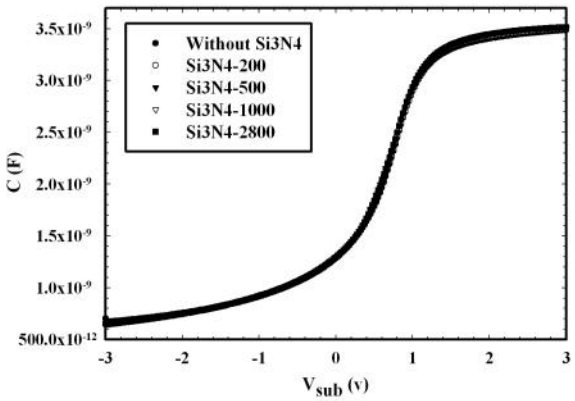

Fig. 3 Measured C-V for different thickness of SiN capping layer.

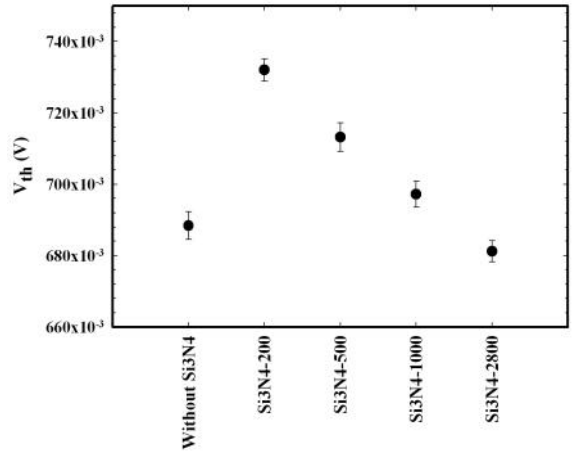

Fig. 4 Threshold voltage for different thickness of SiN capping layer.

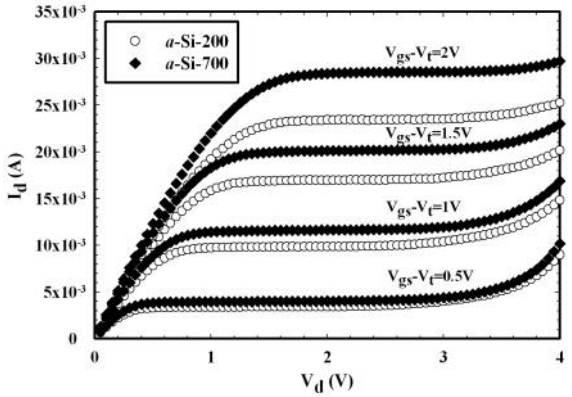

Fig. 5 Output characteristics for different thickness of *a*-Si stack.

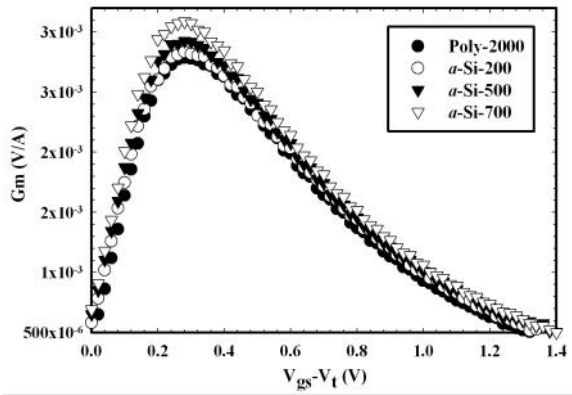

Fig.6 Transconductance for different thickness of *a*-Si stack.

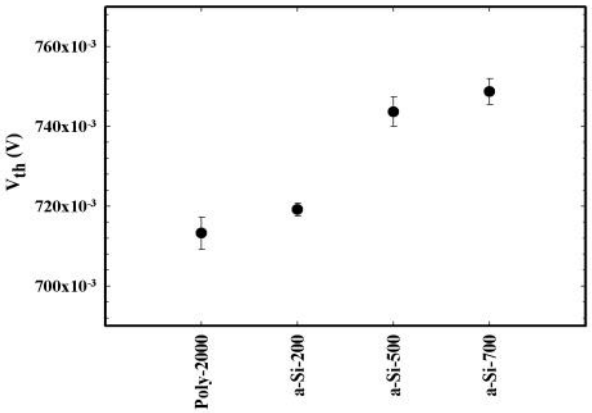

Fig. 7 Threshold voltage for different thickness of *a*-Si stack.

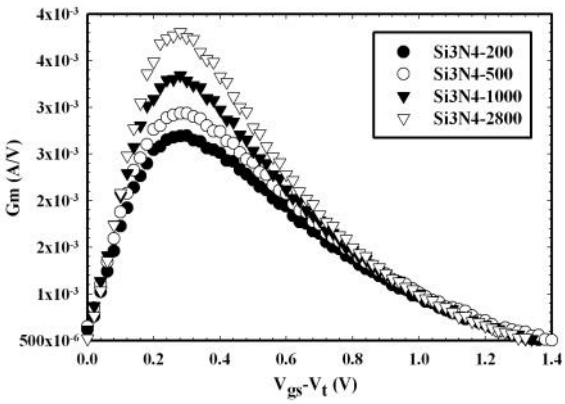

Fig. 8 Transconductance for 50nm *a*-Si layer and different thickness of SiN capping layer.