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Effects of Gate Oxide Scaling and Gate Leakage Currents on Sample and Hold Circuits

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Introduction

RF/mixed mode CMOS has gained much interest recently due to the very high fT of sub-100nm MOSFETs, making many high performance SOC possible. However, as gate oxide is reduced to less than 2nm, gate leakage and the reduced supply voltage can seriously affect many analog circuits such as switch-capacitor or sample and hold circuits. In the case of S/H circuit, the gate leakage current increases the droop rate during the hold cycle and degrades the linearity of the sampled voltage. Fig 1 shows the acceptable droop rate for a given sampling frequency and A-D conversion precision. It is seen that for current state of the art ADC with precision of 10-12 bits and operating frequency of 30-50Mhz, the acceptable limit of the droop rate is a very stringent 10^4V/sec. In this paper, we will examine the effects of gate leakage on the performance of S/H circuits.

Gate Tunneling model.

In order to analyze the effects of gate leakage on S/H circuit, simulation is performed with a 2-D device simulator Medici running in circuit mode. The simple S-H circuit used in the simulation is shown in the Fig. 2 with the transistor (nMOSFET) cross-section shown in Fig. 3 (a). The polysilicon gate devices have a fixed gate length of 50nm and oxide thickness, T_{ox}, in the range of 0.8nm to 1.8nm. Substrate doping is varied to yield a V_{TH} of 0.25Volts. Uniform doping profiles and abrupt junctions were assumed for all the devices. The widths of the NMOS and the PMOS were set at $10\mu m$ and $20\mu m$ respectively to compensate for the mobility difference between the electrons and the holes. The clock voltage applied at the gate of MOSFETs has a period of 300ns (3.33Mhz), a realistic fall time of 5ns and a peak value of 1V. The input voltage is a 0.5V peak to peak 2MHz sinusoid in series with a 0.5V DC signal. The storage capacitor has a value of 0.53pF, which is approximately 10times the total gate capacitance (Cox) of the NFET and PFET, for a Tox of 10Å. The various components of gate tunneling current is shown in Fig. 3 (b) To simulate the gate currents, a calibrated model proposed by Cai, at. el. [1] was used in the simulator. Fig. 4 shows that the model agrees with experimental results [2] over a wide range of gate oxide thicknesses. Similar results are obtained for pMOSFETs

Results and discussion

A number of performance parameters are used in the analysis: (1) acquisition time defined as the time it takes for the voltage on the storage capacitor to reach 99.99% of its final value. T_{acq} improves with smaller Ron by using smaller tox or storage capacitor, both will result in degraded droop rate. (2) Integral nonlinearity, INL, which is the maximum deviation of the S-H output characteristics from a straight line for a linear increase in the input. INL originates from the varying channel resistance for different values of the input voltages. For the quantification of this metric, a varying DC potential was applied to the source of the pass gate and the output was allowed to settle. After this, the pass gate was switched off and the sampled voltage measured. (3) The pedestal voltage which is the error introduced at the S/H output during the transition from sample to hold. This error stems from the channel charge injected by the CMOS switch onto the storage capacitor when the clock voltage turns off. For sub 100nm devices, a part of gate tunneling current also adds to the injected charge on the sampling capacitor. (4) Droop rate which is the rate of discharge of the leakage capacitor during the hold mode. Since transistor parameters such as the gate oxide thickness, bulk doping, the junctions depth, source drain extension length (defined by the angle implant) have opposing impacts on these performance parameters, this paper seeks to quantify the performance trade-offs as different device parameters are varied.

Effect of Gate Oxide Thickness

Since I_D is proportional to Cox, T_{acq} improves with thinner tox device. However, the mobility is degraded due to increase in the vertical electric fields and the substrate doping. Therefore the improvement in the drain current is not linear with respect to gate oxide thickness reduction. Fig. 5 (a) shows the variation of the acquisition time, T_{acq}, with Tox. As it can be seen increasing Cox by 2X only results in about 5% improvement in T_{acq}. Fig. 5(b) shows the droop rate for different oxide thickness, with the gate tunneling model on and off. With the gate tunneling model off, there is a marked improvement with the reduction in Tox because the subthreshold slope improves as the Tox is reduced, leading to smaller leakage currents. However, since the gate tunneling current increases exponentially with reducing Tox, the storage capacitor discharge rapidly through gate leakage for thin Tox device. Fig.(6) shows the affect of gate oxide thickness scaling on the Integral Nonlinearity (INL). The plots, measured 7.5ns after the clock goes to zero, show enhanced nonlinearity due the gate tunneling current. As can be seen, reducing the gate oxide thickness increases the non-linearity in the sampled voltages. This can be attributed to the increase in the channel charge injected (inset of Fig. 6) on the sampling capacitor as the gate oxide thickness is reduced.

Effect of Junction Depth

Ultra-shallow junction is needed to control short channel effects. However, small Xj can lead to an increase in parasitic resistance and therefore an increase in T_{acq} which is not affected by the gate leakage as seen in Fig. 7(a). The rise in the T_{acq} is almost quadratic as the junction depth is reduced. Fig. 7(b) shows the sampled voltage droop rate for various junction depths. The fall in the droop rate is due to the enhanced source drain resistance which reduces the magnitude of V_{GD} and therefore reduces the gate leakage current. Reduction in the droop rate is traded-off with the increase in the T_{acq}; reducing the Xj from 20nm to 8nm increases the T_{acq} by 46.6% whereas the droop rate reduces by 98%.

Effect of Source Drain Extension Length

Fig. 8 (a), show the variation of the T_{acq} with the SDE overlap length, Lov. Reducing Lov increases the $R_{S/D}$ and thus T_{acq}. However, smaller (and negative Lov) can improve the droop rate significantly as shown in Fig. 8 (b) since the dominant gate tunneling current path during the hold mode is via the gate-source overlap region. The inset in Figure 9 shows the variation of the injected charge with the SDE overlap length. In the case of maximum sampled voltage (truce) the charge injection reduces with a reduction in the SDE overlap length, as the total channel current and charge reduces. However, in the minimum sampled voltage (crest) case, the gate tunneling current is reducing the effect of the channel injected charge. This is due to the fact that the tunneling current of the NFET acts to restore the additional charge deposited on the capacitor by the pass gate (mainly pMOSFET due to its larger width). This is particularly true for long Lov where the gate tunneling current is significant. Fig. 9 shows the variation of the INL with Lov. We observe that the INL increases with Lov. Since the overlap capacitance increases with Lov, the charge injected onto the sampling capacitor and hence the nonlinearity increases.

Summary

In this paper, the effects of gate oxide scaling on S/H circuit was examined. As Tox reduces, while T_{acq} improves, the droop rate and the nonlinearity degraded. The excessive gate tunneling current and the reduced mobility are responsible for this behavior. It was shown that since the Xj scaling had only a minor effect on the trade-offs between T_{acq}, droop rate and INL, it should be set by constrains dictated by the ease of fabrication. It was shown that the nonlinearity and the droop rate increase dramatically for FETs with large SDE overlap regions, but only improve T_{acq} marginally. It was concluded that for a sample and hold circuit, small Xj and Lov, with Tox as thick as permitted is desirable.

Reference

[1] J. Cai and C. T. Sah, JAP vol. 89, no, 4, 2001.
[2] C. Choi, et. al, IEEE TED vol. 48, no. 12, 2001.

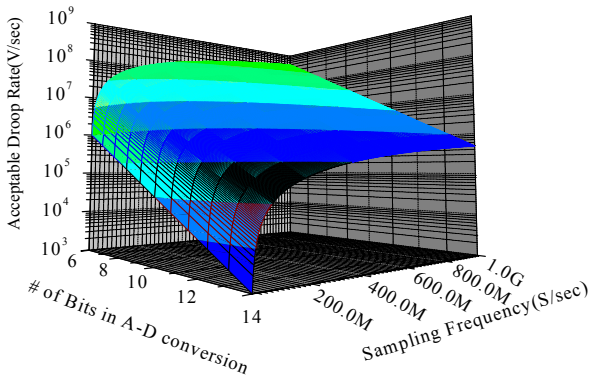

Figure 1. Acceptable droop rates as a function of the A-D converter bit precision and the sampling frequency. The supply voltage is assumed to be 1volts

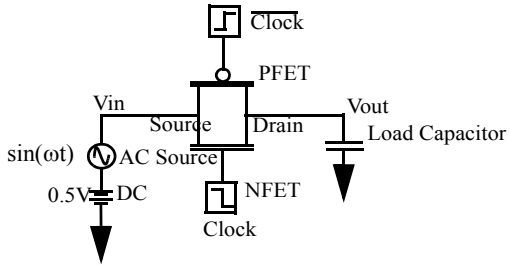

Figure 2. A basic sample and hold circuit. The load capacitances and the power supplies are assumed to be ideal.

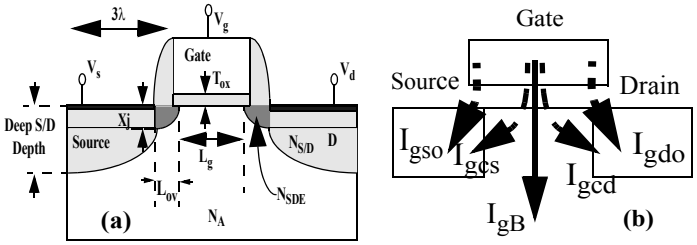

Figure 3. (a) Device structure considered in this study. (b) The various components of gate leakage currents.

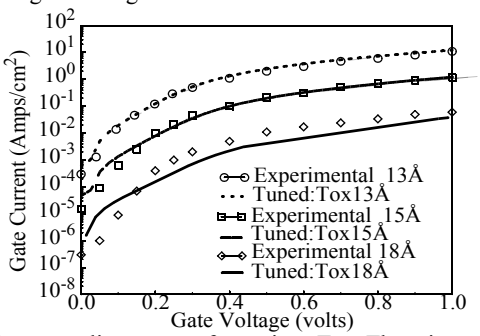

Figure 4: Gate tunneling current for various Tox. There is a good match between the experimental and the simulation data.

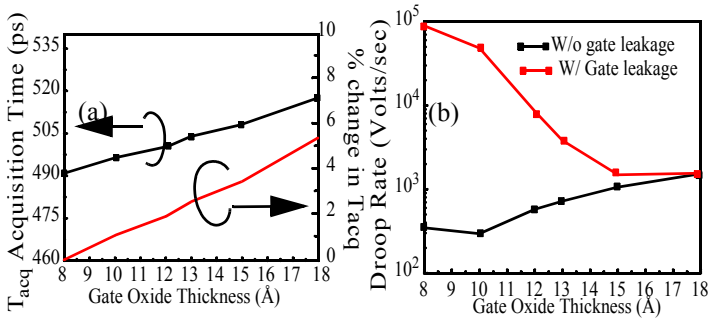

Figure 5: Acquisition time (a) and Hold voltage droop rate (b) as a function of the gate oxide thickness. All the devices had a Vt of |0.25V|.

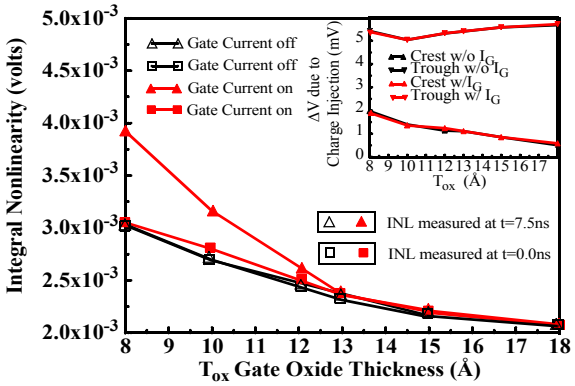

Figure 6: Integral nonlinearity as a function of the gate oxide thickness, all the devices had a Vt of |0.25V|.

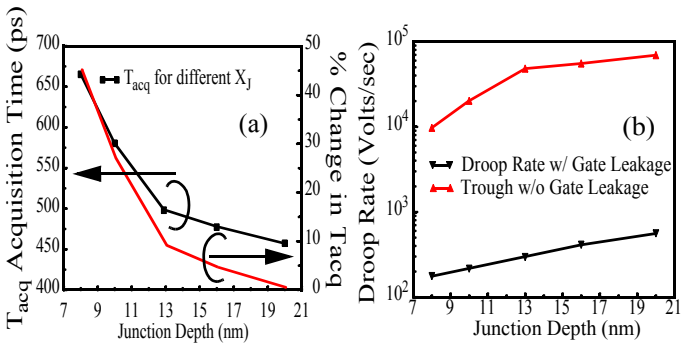

Figure 7: Acquisition time (a) and droop rate (b) as a function of the source drain junction depth, all the devices have a Tox of 10Å and a Vt =|0.25V|.

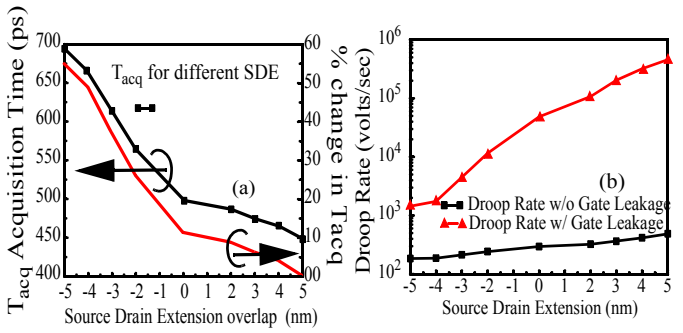

Figure 8: Acquisition time (a) and droop rate (b) as a function of the SDE overlap length, all devices have a Vt of |0.25V|.

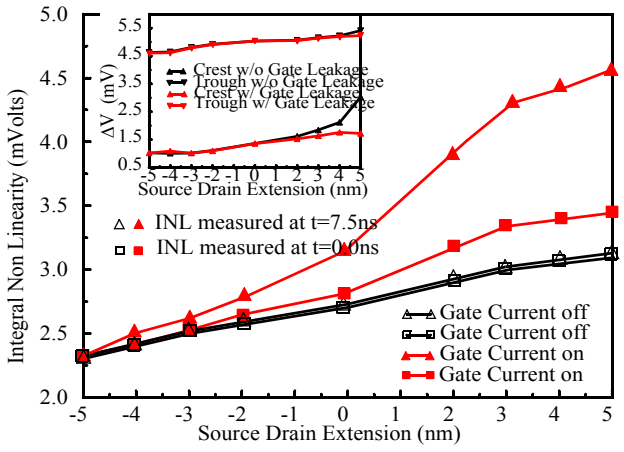

Figure 9: Integral nonlinearity as a function of the SDE length. All the devices had a Vt =|0.25V|.