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Impact of Aggressively Shallow Source/Drain Extensions on the Device Performance

Kenji Kimoto[1], Tetsuya Tada[2] and Toshihiko Kanayama[2]

[1]MIRAI-ASET, AIST Tsukuba Central 4, 1-1-1 Higashi, Tsukuba 305-8562, Japan
Phone: +81-298-49-1599, Fax: +81-298-61-2576, E-mail: kimoto.kenji@mirai.aist.go.jp
[2]MIRAI-ASRC, AIST Tsukuba West 7, 16-1 Onogawa, Tsukuba 305-8569, Japan

1. Introduction

For continued scaling of MOSFETs to the 45-nm technology node (TN45) and beyond, it is becoming increasingly difficult to control the short-channel effects. An obvious way to minimize the short-channel effects is the use of extremely shallow source/drain extensions (SDEs). However, an excessive reduction of SDE depth inherently increases the sheet resistance (R_s) and may degrade the device performance. How to fabricate such a shallow and abrupt junction is also a serious problem. Because of these reasons, the possibility of extremely shallow SDEs has not been fully investigated yet.

In this work, we show by device simulations together with some experimental results that aggressive reduction of SDE depth leads to better performance of bulk MOSFETs for TN45 even if the resulting R_s of SDE becomes higher. In particular, it is demonstrated as an extreme case that a device with SDEs consisting of inversion layers induced by intentionally placed surface charges has sufficient drive current and excellent immunity to the short-channel effects. We call this device structure a charge-transfer-doped SDE MOSFET (CTE-MOS).

2. Device Simulation

Classical 2-D simulations based on a drift-diffusion model were performed using the MEDICI simulator [1] for n-type MOSFETs with n^+ poly-Si gate, with both the gate depletion and physical gate height being neglected.

We considered three types of device structures for the conventional bulk MOSFET (conv.MOS) and CTE-MOS: a high-performance (HP) device with uniformly-doped channel (HP-UD), a HP device with halo regions (HP-HALO) and a low-operating-power (LOP) device with super-steep-retrograde channel (LOP-SSR). The device parameters used here are based on the specifications for TN45 in the ITRS [2] and listed in Table I. The mobility improvement factor specified in the ITRS was not considered. The SDEs of the conv.MOS had box profiles with a concentration of 2×10^{20} cm^{-3}, while the inversion-layer SDEs of the CTE-MOS were formed by placing surface charges with a density of 3×10^{13} cm^{-2} as shown in Fig. 1.

Table I Device Specifications for the 45-nm node

	L_{nom} [nm]	t_{ox} [nm]	V_{DD} [V]	I_{off} [A/μm]
HP	18	0.65	0.6	3×10^{-6}
LOP	22	1.0	0.8	1×10^{-9}

HP: High Performance, LOP: Low Operating Power

The simulation was performed to properly evaluate the device performances, taking into account the short-channel effect on the drive current (I_{on}) as follows [3]. The gate length fluctuation was assumed to be ±20% around the nominal value (L_{nom}). The impurity concentrations of the substrate N_{sub} for HP-UD, the halo regions for HP-HALO, and the SSR region for LOP-SSR, were set so that I_{off} in each case was equal to the I_{off} specification for TN45 at the shortest gate length, L_- (80% of L_{nom}). Then, I_{on} at the longest gate length, L_+ (120% of L_{nom}), which corresponds to the maximum circuit delay, was calculated.

3. Aggressive Reduction of Conventional-SDE Depth

When the SDE depth (X_j) of conventional MOSFETs for HP-UD (Fig. 1 (a)) was reduced from 9.5 nm (the ITRS specified value) to 2 nm while keeping the impurity density of 2×10^{20} cm^{-3}, the I_{on} at L_+ was improved by ~27% although R_s of SDEs increased by ~400% (Fig. 2). This improvement is attributed to two features shown in Fig. 3. One is that the shallower SDE reduced the threshold voltage (V_{th}) shift for the gate length change from L_- to L_+ (ΔV_{th}), leading to the larger gate overdrive at L_+. The other is that the substrate impurity concentration N_{sub} also decreased with SDE depth, resulting in the improvement of the carrier mobility in the channel. Actually as shown in Fig. 4, as X_j was reduced, the decrease of the channel resistance canceled out the increase of the SDE resistance, resulting in the decrease of the total resistance at L_+. Consequently, aggressively shallow SDEs can improve the I_{on} at L_+ in spite of their higher resistance.

We also confirmed that the same conclusion holds for the LOP devices; the I_{on} at L_+ was improved by ~35% when X_j was reduced from 9.5 nm to 2 nm.

4. Performance of CTE MOSFETs

The above results lead to the conjecture that the CTE-MOS which has the inversion-layer SDEs as illustrated in Fig. 1 (b), could exhibit better performances. Thus we estimated the R_s of inversion layer induced by ionized impurities located in SiO_2 layers grown on the Si surfaces. The resulting R_s of electron inversion-layer reaches a minimum value of 2–20 kΩ/□ at a positively-ionized impurity density of around $1–4\times10^{13}$ cm^{-2} (Fig. 5). This is because as the sheet density of the ionized impurity increases, the increase of carrier density competes with the mobility degradation due to the increase of the effective electric field at the interface. We confirmed

experimentally the generation of electron inversion-layers by employing Cs ion implantations into the thermal oxides, as shown in Fig. 5. The observed R_s is close to the simulated values indicating that the n-type CTE-MOS is actually feasible.

On the basis of the above results, we simulated the performance of the CTE-MOS for HP45-UD; the results are compared with those of conv.MOS in Figs. 2–4. These results indicate that the CTE-MOS corresponds to the conv.MOS with ultimately shallow SDEs and shows the best performance among the device structures considered.

We also compared the I_{on} at L+ and ΔV_{th} of the CTE-MOS to those of the conv.MOS with X_j = 9.5 nm for HP-UD, HP-HALO and LOP-SSR (Fig. 6). As seen, the CTE-MOS exhibited the better performance: 1.3 times I_{on} and 1/2.6 of ΔV_{th} for HP-UD, comparable I_{on} and 1/3.5 of ΔV_{th} for HP-HALO, 1.4 times I_{on} and 1/2.6 of ΔV_{th} for LOP-SSR. The similar results were obtained as well for HP-UD and LOP-SSR when the assumption for the gate fluctuation was reduced to ±10%, indicating that the CTE-MOS is an attractive device structure for miniaturized MOSFETs. The inversion-layer SDEs induced by sub-gates were already reported [4]; however, the CTE-MOS is more advantageous in terms of smaller parasitic resistance and capacitance as well as smaller number of process steps.

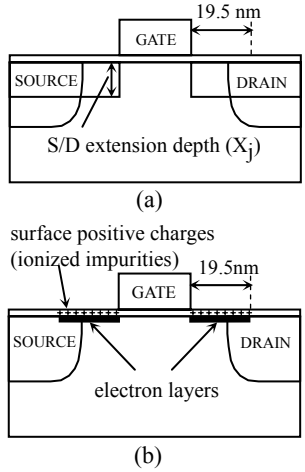

Fig. 1 Schematic structures of the simulated devices for HP-UD:
(a) conv.MOS and (b) CTE-MOS.

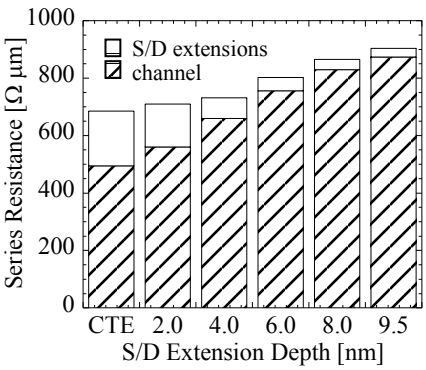

Fig. 4 Series resistance between source and drain regions, divided into the channel and the SDE components.

5. Conclusions

We simulated the drive current of the 45-nm technology node devices, assuming that the gate length fluctuation is ±20% and the maximum I_{off} within the fluctuation should suffice the ITRS specification. As the SDE depth of the conventional MOSFET was reduced under the fixed impurity concentration, the I_{on} at the longest gate length (L+) was enhanced in spite of the SDE resistance increase. This result suggests that the CTE-MOS with inversion layer SDEs is a preferable device structure. Actually, the I_{on} at L+ of the CTE-MOS was larger than that of the conv.MOS. The formation of electron inversion-layers by Cs implanted in SiO_2 confirmed the feasibility of CTE-MOS.

Acknowledgements

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References

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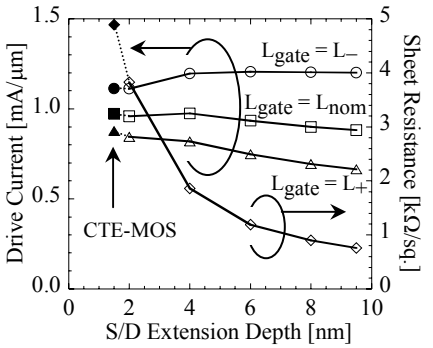

Fig. 2 Drive current and sheet resistance as a function of SDE depth for conv.MOS (open symbols), together with the results of CTE-MOS (solid symbols).

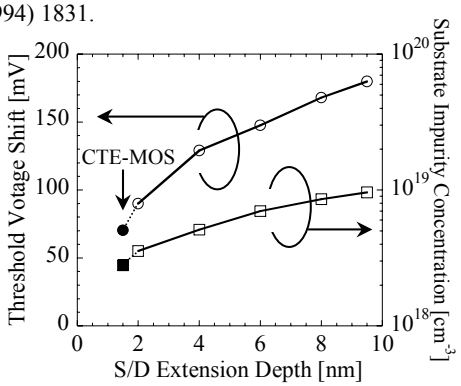

Fig. 3 Threshold voltage shift and substrate impurity concentration (N_{sub}) as a function of SDE depth for conv.MOS (open symbols), together with the results of CTE-MOS (solid symbols).

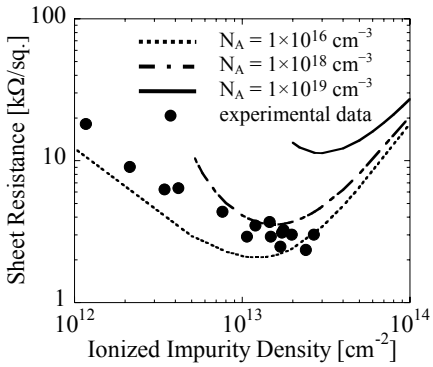

Fig. 5 Sheet Resistance of electron inversion-layers as a function of the ionized impurity density. Results of simulations and experiments using Cs.

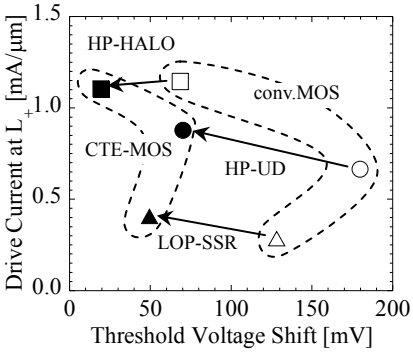

Fig. 6 Relation of drive current at L_+ and threshold voltage shift for three types of conv.MOS and CTE-MOS.