Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 420-421

P2-9

Evaluations of Scaling Properties for GOI MOSFETs in Nano-Scale

G. Du, X.Y Liu*, Z.L.Xia, Y.K Wang, D.Q. Hou, J.F. Kang, R.Q. Han
Institute of Microelectronics, Peking University, Beijing 100871, China
***Tel:8610-62756745, Fax:8610-62757761, E-mail:xyliu@ime.pku.edu.cn**

1. Introduction

Ge MOSFET's have attracted tremendous attention due to the high carrier mobility especially in the low-field. Significant performance improvements of Ge MOSFET have been reported for the long channel devices [1,2]. Compared to Si, in bulk Ge the velocity would saturate at a lower field with a lower saturation velocity. Thus the scaling behavior of Ge MOSFET with gate length in nano-scale is very important. In the other hand, sub-100 nm Ge n-MOS devices have been investigated by some theoretical approaches within the Non-Equilibrium Green's Function formalism, most of which are based on the ballistic simulation and constant effective mass approximation [4-6]. But all of those works assumed an unrealistically high mobility in the source. Hence, it is not clear of the Ge MOSFET scaling behaviors in the nano-scale in which the electric fields are rather strong and with Ge/dielectric interface. In this work for the first time, characteristics of both n- and p-channel GOI MOSFETs with channel length (L_{ch}) ranging 20nm ~ 130nm are simulated by 2D self-consistent full-band MC device simulator to investigate the scaling properties. The drive current and subthreshold characteristics are investigated for various channel length and Ge layer thickness.

2.Devices Design and Simulation

The performance of both n- and p- GOI MOSFETs with L_{ch} varying from 20nm to130nm are simulated on Ge <100> substrate using the parameters listed in table 1. The schematic structure of a GOI n-MOSFET studied in this work is shown in Fig.1. The devices are optimized to have same leakage currents with various channel length. The full band structure of Ge is obtained from empirical pseudopotential calculation including spin-orbit interactions [7]. The transition rates for the various scattering processes are calculated based on Fermi's Golden rule. The acoustic and optical phonon scattering, the ionized impurity scattering, and the impact ionization scattering are also taken into account [8,9]. The deformation potentials of Ge used in the work are the same as described in ref. [10]. The surface roughness effect is considered as one of the additional scattering mechanisms, similar to what has been done in Si device [11].

3. Drive Current and Intrinsic Performance of GOI Devices

Fig.2 plots the dependence of intrinsic performance $C_g V_g/I_{on}$ on Ioff both for n and p-GOI MOSFETs at |Vds|=1V with various channel length. Fig.3 shows the ratio of pMOS and nMOS intrinsic delay $\tau p/\tau n$. From the figures, it can be found that both n and p channel GOI MOSFETs have favorite intrinsic performance in nano scale even with lower saturation velocity at a lower field. It is also interested to note that the p-MOSFETs become closely comparable to that of n-MOSFETs due to the relatively stronger non-stationary effect for holes. Thus p channel GOI MOSFET will have much more favorable drive current scaling behavior in nano-scale. Fig. 4 and 5 suggest that when L_g is scaled to below 50 nm, the carriers velocities overshoot region extends from drain to source and becomes larger than the saturation velocity. This explains why I_{DS} would still increase despite the stationary velocity would saturate at a lower field with a lower saturation velocity in Ge . Thus the drive current as well as the intrinsic performance will increase with reduction of channel length. Fig.6 plots the electron velocity distribution along the channel (in y direction) with various channel depth for 20nm GOI pMOSFET. Due to the surface roughness scattering, the velocity near the surface is reduced especially near source side even with obviously velocity overshoot. Thus the surface roughness scattering might suppress the non-stationary transport and Ge/dielectric interface is still an important issue in ultra-short MOSFET.

4. Subthreshold Characteristics and Short Channel Effect

The SCE is investigated for both n and p channel GOI MOSFET as shown in Fig.7,8,9 with various Ge layer thickness T_{Ge}. From the figures, it can be seen that the Vth roll-off and S factors are ratio to T_{Ge}/Lch both for n and p MOSFET with various channel length. Reducing T_{Ge} can minimize SCE. Since the dielectric constant εs of Ge is 16 and larger than Si (11.9). Thus the coupling between source and drain becomes serious and also cause worse SCE in Ge. From the simulation results, it can be found that the Vth roll-off and S factors can be optimized by $T_{Ge}=L_{ch}/4$. And this follows the scaling theory in Si UTB devices if changing the dielectric constant of Ge. Hence, scaling GOI devices the SCE is also a critical issue.

5. Conclusion

Self-consistent full band MC simulation is used to investigate the drive current scaling properties of GOI CMOSFETs. The results indicate that both for n and p channel GOI MOSFETs have favorable scaling properties in nano-scale due to the non-stationary transport near source side especially for p channel device. But the surface roughness scattering is a critical issue that might suppress the non-stationary transport. SCE is serious in GOI devices and much thinner Ge layer have to use to optimize the performance.

* This work is supported by G200036502.

Reference

1.Chi On Chui et al., IEDM Tech. Dig., 2002, p437 2. Huiling Shang et al. IEDM Tech. Dig., 2002, p441 3. S.M.Sze, Physics of semiconductor devices, John Wiley & Sons, Inc, 1985 [4].Tony Low, et.al., VLSI Tech.2003, p117 [5].Anisur Rahman, Avik Ghosh and Mark Lundstrom, IEDM 2003 [6].Tony Low, et.al., IEDM 2003 [7].J. R.Chelikowsky and Marvin L. Cohen, Phys. Rev. B v.14, 556, 1976 [8].Carlo Jacoboni and Lino Reggiani, Review of Modern Physics, vol.55, No.3, 1983, p645 [9].Phuong Hoa Nguyen, Karl R.Hofmann and Gernot Paasch, J. Appl. Phys. 94(1), 2003, p376 [10].F.M.Bufler, et.al, IEEE Trans. Electron Devices Vol.50, No.2, p418, 2003 [11] C.Jungemann, Stefan Keith, Martin Bartels, and Bernd Meinerzhagen, , IEICE Trans. Electron., Vol. E82-C, No.6, 870-879, 1999

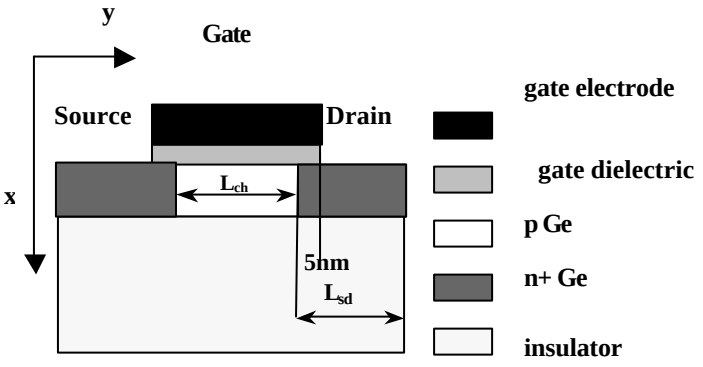

Fig. 1 The schematic structure of a GOI n-MOSFET. Ge <100>, and $N_{S/D}=2x10^{19}cm^{-3}$, the other parameters are listed in table 1.

Table 1 Parameters of GOI n and p MOSFETs

L_{ch} (nm)	T_{Ge} (nm)	N_{ch} (cm^{-3})	EOT (nm)	L_{sd} (nm)
20	5	$5x10^{17}$	0.8	30
45	11.25	$1x10^{17}$	1	55
65	16.25	$7x10^{16}$	1.2	75
90	22.5	$3x10^{16}$	1.5	100
130	32.5	$1x10^{16}$	1.8	140

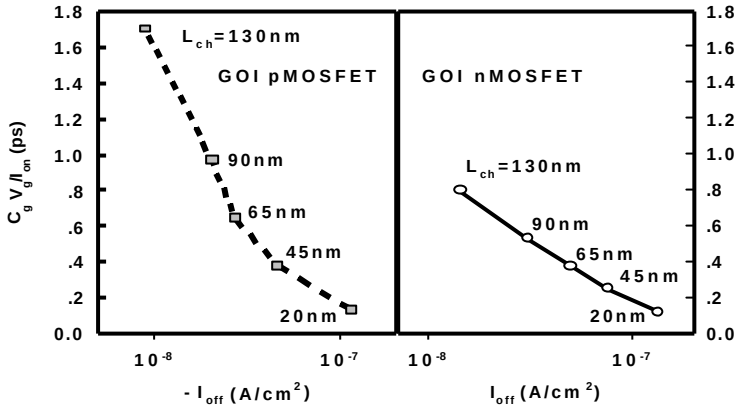

Fig.2 the dependence of intrinsic performance CgVg/Ion on Ioff both for n and p-GOI MOSFETs at |Vds|=1V with various channel length.

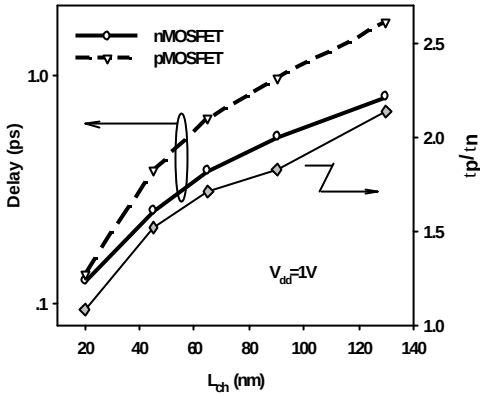

Fig.3 the ratio of pMOS and nMOS intrinsic delay τp/τn.

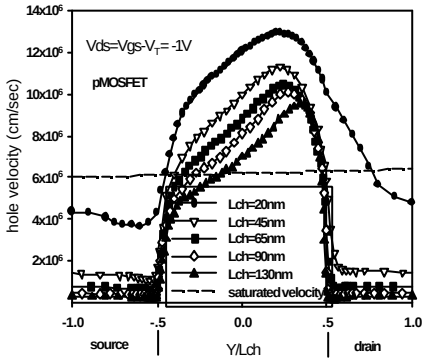

Fig.4 The average holes velocities distribution in p- MOSs with various L_{ch} along the channel.

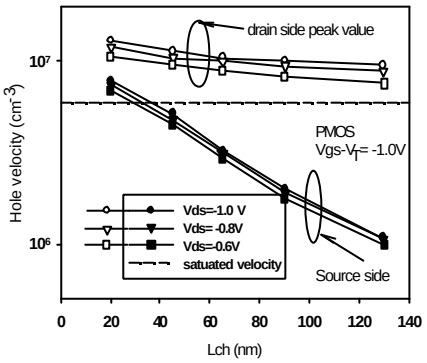

Fig. 5 The average holes velocities at the the potential barrier near source side and drain side peak velocities with various $L_{ch.}$

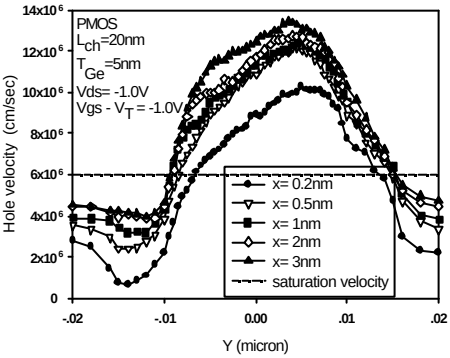

Fig.8 The hole velocity distribution along the channel (in y direction) for various channel depth (in x direction) for 20nm GOI pMOSFET.

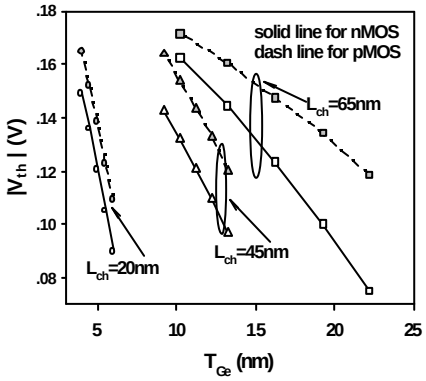

Fig.7 The dependence of Vth to the T_{Ge}

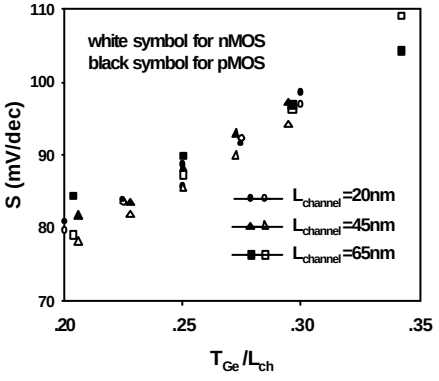

Fig.8 The dependence of S factor to the T_{Ge}/L_{ch}

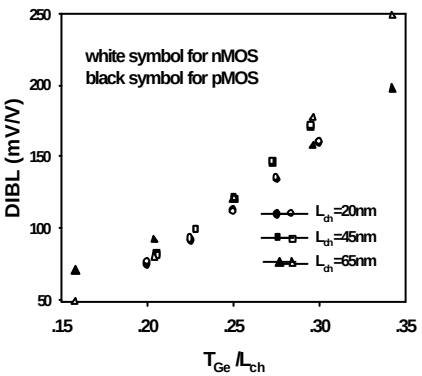

Fig.9 The dependence of DIBL to T_{Ge}/L_{ch}