Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 446-447

P3-1

The development of TiN Bottom Electrodes Isolation Methods for the Fabrication of sub-micron DRAM Capacitor

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1. Introduction

One of the most critical challenges to sub-micron dynamic random access memory (DRAM)'s face is memory cell capacitance. Recently, extensive approaches have been reported to ensure a sufficient capacitance in a limited area for a DRAM development. The robust stack storage node (SN) and sufficient cell capacitance for high performance are inevitable for sub-micron DRAM capacitance process [1-4]. In this article, the technology of titanium nitride (TiN) bottom electrode isolation using blanket dry etch for the fabrication of sub-micron DRAM capacitor is proposed and developed, which can be extended to the next generation DRAM fabrication.

TiN is one of the most reliable candidate in electrode materials of sub-micron DRAM capacitor. Generally, the following bottom electrode isolation processes are widely used in DRAM memory cell capacitance fabrication area.

(a) PR coating → Shallow Blanket Expose → Dry Etch
(b) PR coating → TiN isolation using CMP
(c) PR coating → PR Etch → Dry etch

The above conventional processes for a formation of bottom electrode isolation commonly use Photo Resist (PR) as dry etch or CMP (Chemical Mechanical Polishing) barrier for isolation of bottom electrode. However, some critical problems exist in all the above processes. Because all of the above processes utilize PR as barrier for isolation of bottom electrode, they inevitably have to use expose & develop equipment of photo lithography area and PR Striper following dry etch process or CMP process, which prolongs process time and complicates fabrication process. Another problem is that PR residue following PR strip process or anneal & dip out process becomes the source of large amount of defect, which lead to fatal problems such as single or multi bit fail. Consequently these problems reduce the yield of mass production.

New method of bottom electrode isolation without using barrier film such as PR is needed. Without using any barrier materials and CMP process, TiN bottom electrode isolation method is successfully developed using blanket dry etch process with Cl_2 and Ar mixed gas discharges. Hereafter, this process is referred to as barrierless etch process.

2. General Instructions

The cross sectional structure image of our 80nm DRAM cell capacitor is illustrated in Fig. 1. The stack height of 1.8 μm double oxide layers such as PETEOS (Plasma Enhanced Tetra-Ethyl-Ortho-Silicate) and PSG (Phosphorous Silicate Glass) with different wet etching rates are deposited on the Si_3N_4 layer that served as the etch stopping layer during the storage node fabrication. The double layer oxide films are etched by anisotropic etching. The area of the SN is enlarged due to a different wet etch rate being used during the pre-cleaning process. After that, Ti as a barrier metal and TiN film as a SN bottom electrode are deposited for formation of SN bottom electrode. Then, dry etch process using Cl_2 and Ar mixed gas discharge is performed in order to isolate the TiN bottom electrode films.

The top view defect image as illustrated in Fig. 2 can be easily observed when conventional processes are adopted for a fabrication of bottom electrode isolation, such as PR barrier dry etch process or PR barrier CMP process. The defects are frequently observed in these conventional processes, which can lead to single or multi bit fail, electrically. However, Fig. 3 shows the defects are remarkably reduced when barrierless etch process is used. We have come to the conclusion that PR residue from bottom electrode isolation process directly influences single or multi bit fail.

The illustrations in Fig. 4 compare the results of PR barrier bottom electrode isolation process with those of barrierless process. There is no difference in both processes as seen from the top view and cross sectional SEM image. The amount of TiN loss after barrierless TiN bottom electrode etch process is less than 50Å as illustrated in Table 1. In other words, TiN attack almost does not occur during the bottom electrode isolation process using blanket dry etch.
As shown in Fig. 5 and Fig. 6, leakage current characteristics of SN with barrierless etch process is same or slightly superior to those of SN with PR barrier process. Memory cell capacitance Cs also has similar results in both processes.

3. Conclusions

For the first time, we successfully demonstrated TiN bottom electrode isolation process without conventional PR barrier process for 80nm MIM capacitor. The electrical characteristics of SN such as memory cell capacitance Cs, leakage current, and breakdown voltage from both barrier-

less etch process and PR barrier process show almost no difference. On the other hand, the defects are remarkably reduced when barrierless etch process is used. With barrierless etch process, we have solved some serious problems of PR barrier bottom electrode isolation process as mentioned above. As a result of our study, we reduced the amount of defect and simplified process by reducing process steps, thus developing a reliable bottom electrode isolation process in DRAM fabrication.

Acknowledgements

We would like to express our appreciation to all the members of the Advanced Process – 1 Team, at HYNIX Semiconductor Inc. for their contribution to this study. This work is supported by the Memory R & D Division at HYNIX Semiconductor Inc.

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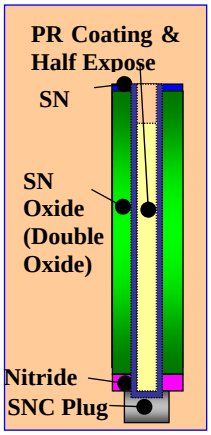
Figure Caption



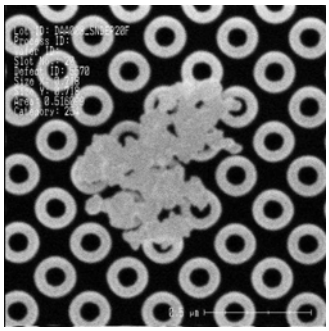


Fig. 2 Top view defect image from conventional bottom electrode isolation process

Fig. 1 The cross sectional structure diagram of 80nm DRAM cell capacitor

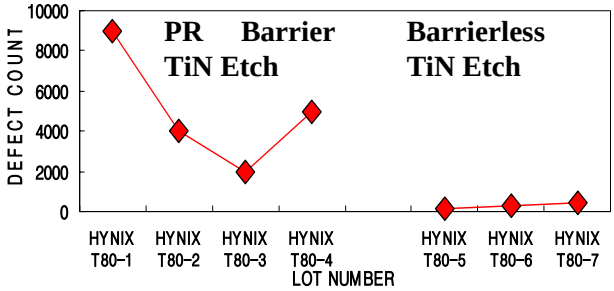


Fig. 3 The defect trend comparison between the results of PR barrier isolation process and those of barrierless process.

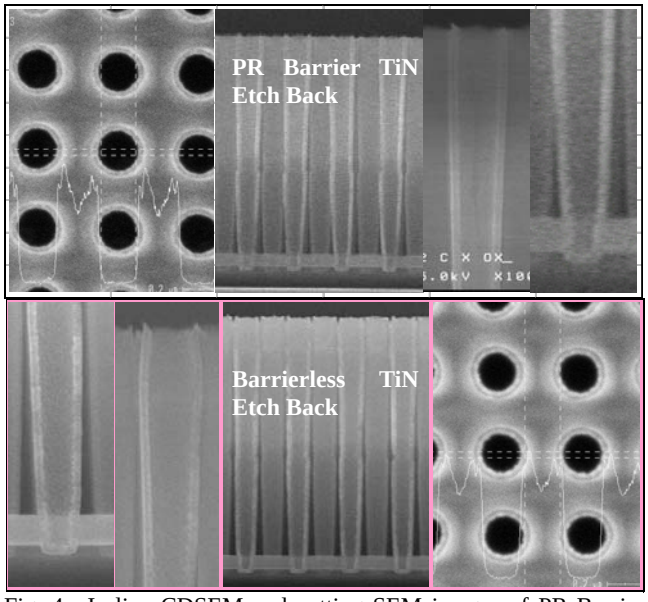


Fig. 4 In-line CDSEM and cutting SEM images of PR Barrier and barrierless isolation profile

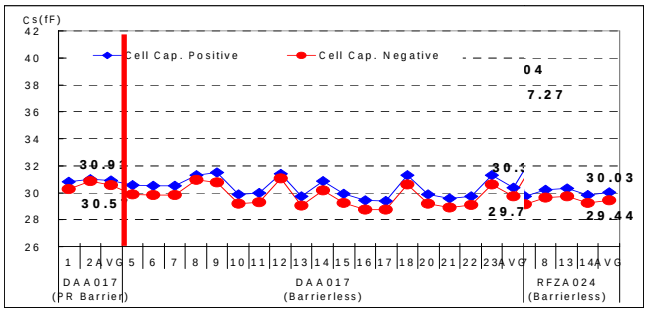


Fig. 5 Memory cell capacitance Cs trend of PR barrier process and barrierless process

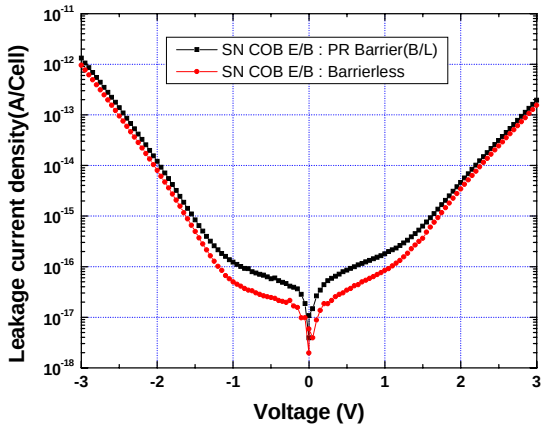


Fig. 6 Leakage current characteristics of SN with PR barrier process and barrierless process.

R_TiN	LB	LBC	C	RTC	RT	Avg	3-Sig
Top	-	285	285	306	346	**306**	**25**
Middle	-	367	326	347	367	**352**	**17**
Bottom	326	346	367	367	346	**350**	**15**

Table 1 TiN Loss after barrierless bottom electrode isolation process (Unit : 10^{-10}m)