Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 466-467

P3-11

Poly-Si Comparable Fermi-Level Pinning of Fully Silicided Platinum Gates on HfO_2

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1. Introduction

Fully silicided metal (such as NiSi) gate electrodes have gained considerable attention for the metal gate electrodes in scaled CMOSFETs [1,2]. They have some advantages of continuing the conventional process such as processing using poly-Si gate electrodes. However, high effective work functions for pMOSFETs have not been obtained using NiSi electrodes. Furthermore, the behavior of the effective work function ($\Phi_{m,eff}$) on HfO_2 dielectrics has not been investigated yet, while shifts in V_{FB} on HfO_2 dielectrics were reported using p^+poly-Si gate electrodes and interpreted in terms of Fermi-level pinning [3-7]. In this paper, for the first time to our knowledge, we have investigated the fully silicided platinum (PtSi) as a possible gate electrode for pMOSFETs and demonstrated the Fermi-level pinning on HfO_2 using these electrodes.

2. Experimental

The process flow of the PtSi gate MOSCAPs is summarized in Fig. 1. Thermal SiO_2 or ALD-HfO_2 films on SiO_2 were used for the gate dielectrics. 100 nm-thick undoped amorphous-Si (a-Si) films were deposited at 540ºC on the gate dielectrics. High temperature annealing was typically carried out at 950ºC in order to simulate the activation annealing of dopants in the conventional process. 100 nm-thick platinum films were deposited by DC magnetron sputtering on the poly-Si layer. The gate electrodes were silicided at 400ºC and then annealed in a hydrogen ambient at 400ºC.

3. Results and Discussion

3.1 $\Phi_{m,eff}$ of PtSi on SiO_2

Fig. 2 shows the cross-sectional TEM images of the gate electrode structures (a) before and (b) after silicidation annealing. It seems that platinum atoms uniformly reached the SiO_2 top interface during silicidation annealing. We also confirmed that platinum mono-silicide phase was formed near the SiO_2 interface by RBS analysis. Furthermore, as shown in Fig. 3, high-frequency (HF) C-V characteristics depend on the measured frequency before silicidation, while they are independent of frequency after silicidation. This fact also confirms that the PtSi gate electrode was fully formed to the SiO_2 top interface by the silicidation annealing at 400ºC.

Fig. 4 shows HF C-V curves of PtSi gate MOSCAPs with 3.5, 5.5 and 8.5 nm-thick SiO_2 using n and p-type substrates. No frequency dependence in the C-V is observed regardless of SiO_2 thickness and substrate type. Moreover, no gate depletion effect is observed. The $\Phi_{m,eff}$ of PtSi gate electrode is determined to be about 4.9 eV from the extrapolation of V_{FB} vs. EOT plot as shown in Fig. 5. It implies that PtSi gate electrode is a promising candidate as the metal gates for SiO_2 pMOSFETs.

3.2 Large Shifts in $\Phi_{m,eff}$ on HfO_2

A HF C-V curve of PtSi gate MOSCAPs with 4 nm-thick HfO_2 dielectrics is shown in Fig. 6. A large shift in V_{FB} by about 0.3 V is observed towards the negative direction. This negative shift is located within the gray area in Fig. 7, which is consistent with V_{FB} shifts in the literatures for poly-Si gate electrodes [3-7]. This shift towards the mid-gap indicates that Fermi-level pinning occurs in the HfO_2 top interface and determines the $\Phi_{m,eff}$ value of the PtSi gates, even though a finite shift due to fixed charges in HfO_2 is taken into consideration.

In order to investigate the impact of the a-Si/HfO_2 interface on $\Phi_{m,eff}$ of the PtSi gates, we compared the V_{FB} of PtSi gate MOSCAPs with HfO_2 which were subjected to annealing at various temperatures before depositing platinum films. Since PtSi gate can be formed at the low temperature of 400ºC unlike poly-Si gates, a thermal effect on the Fermi-level pinning was studied. Fig. 8 shows that the extent of negative V_{FB} shifts of MOSCAPs with HfO_2 from those with SiO_2 remains unchanged irrespective of annealing temperatures, while V_{FB} shows a very small dependence on the annealing temperature. The activation annealing does not play an important role in the Fermi-level pinning on HfO_2. This suggests that strong Fermi-level pinning occurs at the PtSi/HfO_2 interface regardless of the maximum process temperature. It is likely that the tendency of Fermi-level pinning at the PtSi/HfO_2 interface is similar to that at the poly-Si/HfO_2 interface as shown in Fig. 7. Further investigation about the role of platinum atoms in the HfO_2 top interface is required in order to fully understand the mechanism of Fermi-level pinning at the PtSi/HfO_2 interface.

4. Conclusion

We have demonstrated for the first time that PtSi gate electrodes which have the high $\Phi_{m,eff}$ of about 4.9 eV as a possible metal gate electrode for pMOSFETs with SiO_2. However, Fermi-level pinning at the PtSi/HfO_2 interface is observed and almost independent of the maximum process temperature. It is likely that the Fermi-level pinning at the PtSi/HfO_2 interface is comparable to that at the poly-Si/HfO_2 interface.

Acknowledgments

This work was supported by NEDO.

References

[1] J. Kedzierski et al., IEDM Tech. Dig., 2002, p. 247.
[2] W. P. Maszara et al., IEDM Tech. Dig., 2002, p. 367.
[3] S. Pidin et al., Symp. on VLSI tech., 2002, p. 28.

[4] C. W. Yang et al., Appl. Phys. Lett., **83** (2003) 308.
[5] C. Hobbs et al., Symp. on VLSI tech., 2003, p. 9.
[6] T. Sasaki et al., Extended Abstracts of IWGI 2003, p. 20.
[7] V. S. Kaushik et al., Extended Abstracts of IWGI 2003, p. 62.

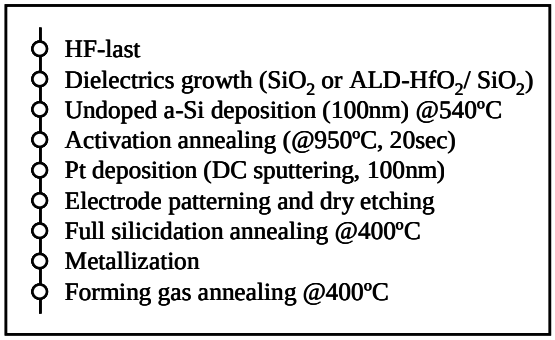

Fig. 1 Fabrication process of fully silicided platinum gate MOSCAPs.

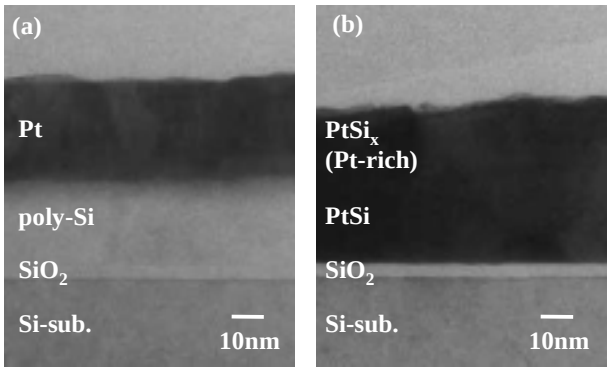

Fig. 2 Cross-sectional TEM images of the gate electrode structures: (a) before and (b) after silicidation annealing. PtSi phase was formed on the SiO_2 interface layer after silicidation annealing at 400ºC.

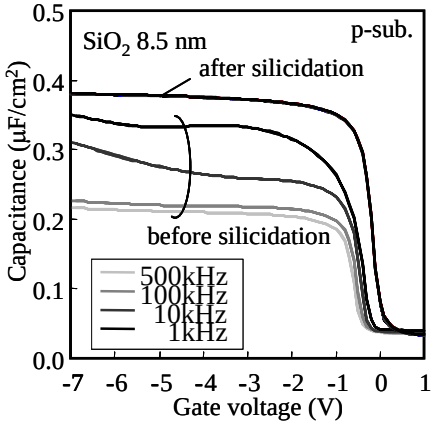

Fig. 3 Comparison of HF C-V curves for PtSi gate MOSCAPs before and after silicidation annealing. HF C-V measurements were carried out at 1k, 10k, 100k and 500kHz. Frequency dependence disappears after silicidation annealing.

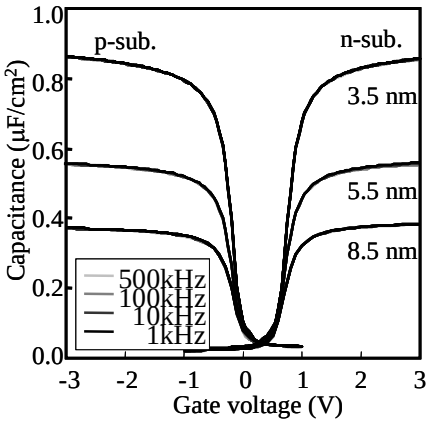

Fig. 4 HF C-V curves of PtSi gate MOSCAPs with 3.5, 5.5 and 8.5 nm-thick SiO_2 on n and p-type substrates. No frequency dependence is observed for all PtSi gate MOSCAPs.

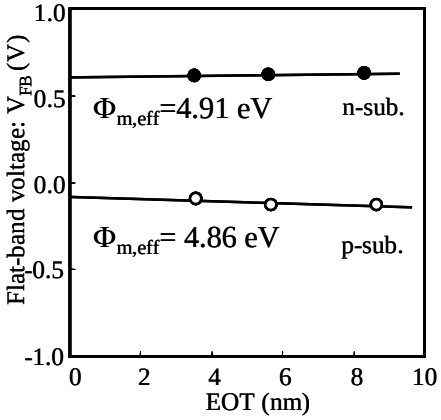

Fig. 5 V_{FB} as a function of EOT for PtSi gate MOSCAPs with n and p-type substrates. The effective work function of PtSi gate electrodes is about 4.9 eV regardless of substrate type as estimated from the extrapolation to y-axis.

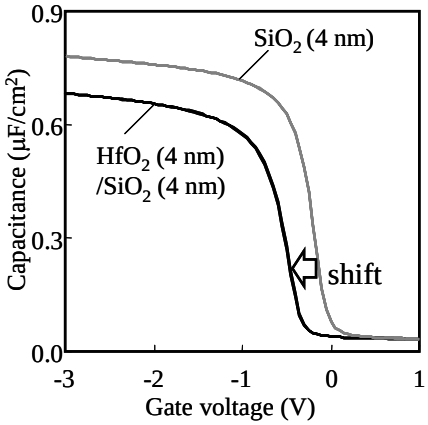

Fig. 6 Typical HF C-V curve for PtSi gate MOSCAPs with HfO_2/ SiO_2 gate dielectrics. V_{FB} is shifted about 0.3 V towards the negative direction by inserting the HfO_2 layer between PtSi and SiO_2.

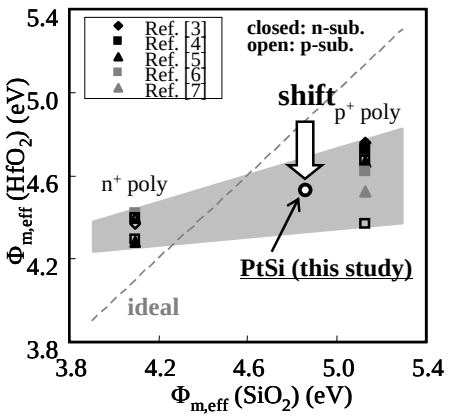

Fig. 7 Comparison of the effective work function between PtSi and poly-Si gate electrodes [3-7]. The effective work function of PtSi is shifted to about mid-gap of Si (gray area) which is expected from the reported shifts in V_{FB} using poly-Si gate electrodes.

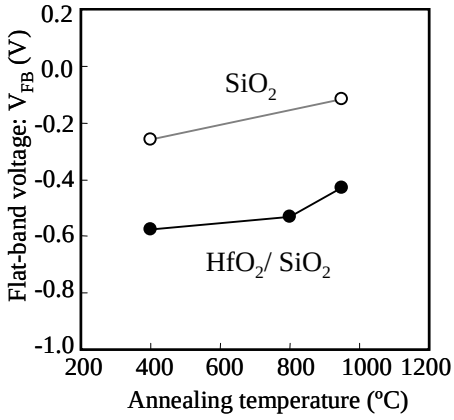

Fig. 8 V_{FB} as a function of annealing temperature. The extent of negative V_{FB} shifts of PtSi gate MOSCAPs with HfO_2 from those with SiO_2 remains unchanged irrespective of annealing temperatures.