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Optimization Technique of Number of Interconnect Layers and Circuit Area Based on Wire Length Distribution

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1. Introduction

This paper discusses the relationship between Si CMOS ULSI circuit area and the number of interconnect layers on the basis of **W**ire **L**ength **D**istribution (WLD); the relationship has a quite important impact because it is directly related to fabrication and manufacturing cost. Using WLD which give a relation between a number of interconnect wire and its lengths, several attempts on chip performance predictions have been reported [1-3].

In this paper, we propose a methodology to optimize a number of interconnect layers and circuit area of Si ULSI.

2. Wire Length Distribution

Figure 1 shows a example of **W**ire **L**ength **D**istribution (WLD). Circles (O) show data from a macro block of a commercially available 0.13μm technology node CMOS chip. The broken line is the distribution calculated from analytic expression [1], while the solid line is calculated with the core utilization consideration [3]. The parameters required for depicting the distribution are number of gates N_{gate}, Rent's constans of p and k, and core utilization. In general, complex circuits tend to have large p and small k, while simple circuits have small p and large k. The core utilization ($\boldsymbol{U}$) is defined as $\boldsymbol{U}$=(cell area)/(circuit area). The method to determine p, k, and $\boldsymbol{U}$ has been reported by the authors [3]. It is noted that the parameters required for representing WLD are the number of gates N, Rent's constant of p and k, and the core utilization of $\boldsymbol{U}$. The operation frequency $\boldsymbol{f}_c$ is estimated by the equation indicated in Fig. 1 [4].

3. Relation between Circuit Area and Number of Interconnect Layer

Circuit specification evaluated is summarized in Table 1. The specification is equivalent to 0.18μm technology. One million gates are assumed to be integrated on 10mm^2 area if the core utilization $\boldsymbol{U}$ is 100%; an average gate area is 3.2×3.2μm^2. The circuit area varies depending on the core utilization; $\boldsymbol{A}_{circuit} \propto 1/\boldsymbol{U}$. As interconnect structure, one-tier structure is assumed, *i.e.*, every interconnect layer has the same metal cross section and interlayer dielectric thickness. The assumption of one-tier interconnect is supposed that the following results and discussion are relating to macro blocks of a chip. The values of interconnect capacitance and resistance C_{int} and R_{int} that are calculated by ref .[5] are dependent on WLD and the core utilization.

Figure 2 shows a operating frequency $\boldsymbol{f}_c$ as a function of chip area. For simple circuits (p= 0.5 and 0.6), $\boldsymbol{f}_c$ is improved in the small circuit area region because of the decrease of resistance. On the other hand, the complex circuits (p= 0.7 and 0.8) have a optimum area to have maximum $\boldsymbol{f}_c$ [3]; the decrease of $\boldsymbol{f}_c$ at small $\boldsymbol{A}_{circuit}$ is attributed from the increase of line-to-line capacitance, and decrease of $\boldsymbol{f}_c$ at large $\boldsymbol{A}_{circuit}$ is attributed from the increase of wire resistance. Figure 3 shows $\boldsymbol{f}_c$ as a function of $\boldsymbol{A}_{circuit}$ for complex circuits (p= 0.8). Parameter is the number of interconnect layers $\boldsymbol{n}$. $\boldsymbol{f}_c$ has the maximum value; the reason is the same as in Fig. 2. From Fig. 3, if the required operating frequency is 230MHz, we have several choice as indicated by $\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$ in Fig. 3; the choice is summarized in Fig. 4. Figure 5 shows the relationship between circuit area $\boldsymbol{A}_{circuit}$ and the number of interconnect layers $\boldsymbol{n}$ to achieve the highest circuit operating frequency. For simple circuits, $\boldsymbol{A}_{circuit}$ does not change to achieve highest $\boldsymbol{f}_c$ with increase of $\boldsymbol{n}$, while $\boldsymbol{A}_{circuit}$ and $\boldsymbol{n}$ has a close correlation.

Chip cost $\boldsymbol{C}$ is considered to have the relation; $\boldsymbol{C} \propto (\boldsymbol{A}_{circuit} \times \boldsymbol{n}^{\alpha}) / \boldsymbol{f}_c^{\beta}$, where α is the process dependent parameter and β may be market determined parameters. One will be able to correlate the WLD which is one of design data information with process and manufacturing cost.

4. Conclusions

This paper discusses the relationship between the number of interconnect layers and the circuit area on the basis of the WLD model. It has been shown that there exists the optimum chip area and the number of interconnect layer to achieve the required operating frequency. We have shown the possibility to make a relationship between design data of WLD and process/manufacturing cost. In the advanced process development the co-design concept of circuit design and process development becomes important for cost effective manufacturing.

Acknowledgements

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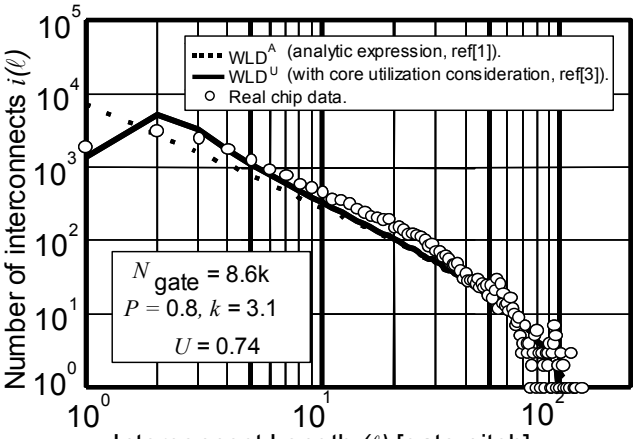


$$f_C = 1\Big/\left[f_{ld} \times \left\{ \begin{matrix} R_{gout}\, fout\left(0.86 \cdot C_{int}\, \ell_{av} + 0.86 \cdot C_{gin}\right) \\ + R_{int}\, \ell_{av}\left(0.37 \cdot C_{int}\, \ell_{av} + 0.86 \cdot C_{gin}\right) \end{matrix} \right\} \right]$$

ℓ_{av}: average intcnt length
R_{int}: intcnt resistance per unit length
R_{gout}: gate output resistance
C_{int} : intcnt capacitance per unit length
C_{gin} : gate input capacitance
f_{ld} : logic depth

Fig. 1. Wire **L**ength **D**istribution (WLD) and the prediction of operating frequency f_c.

Table 1 Circuit Specification (Equivalent to 0.18μm node).

Number of Gates	10^6
Chip Area @***U***=100%	10mm^2 (10μm^2/gate)
Rent's parameters (p, k)	(0.8, 2), (0.7, 2.5), (0.6, 3), (0.5, 3.5).
Intcnt cross section	one-tier multilevel intcnt metal cross section: 0.2μm×0.2μm metal spacing; dependent on ***U*** ILD thickness: 0.2μm (ε = 3.9)
R_{gout}, C_{gin}, and f_{ld}	4 kΩ, 2.1fF, and 20

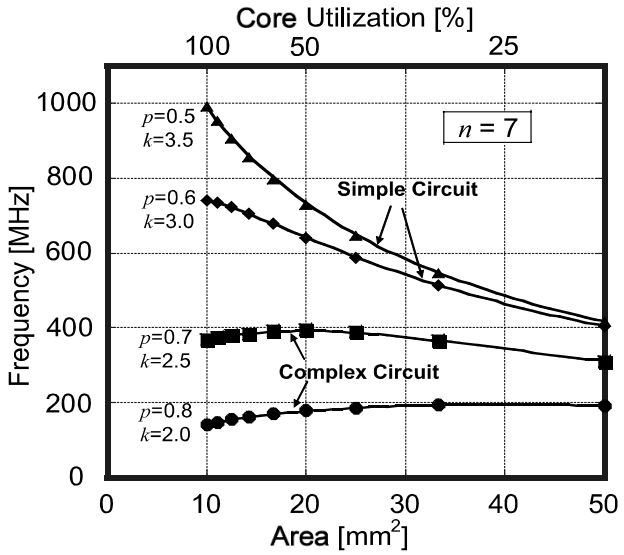


Fig. 2. Operating frequencies as a function of circuit area.

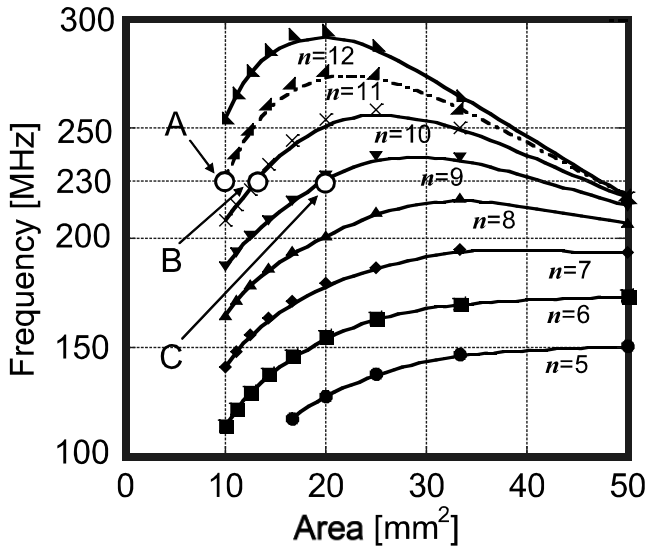
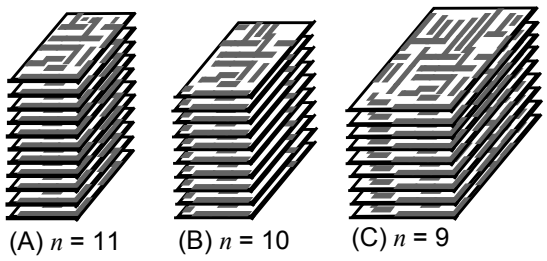


Fig. 3. Operating frequencies for complex circuit (p=0.8).



	A	B	C
Operating freq. f_c	230 MHz		
Circuit Area $A_{circuit}$	10 mm^2	12.5 mm^2	25 mm^2
# of intcnt layers ***n***	11	10	9

Fig.4. Choices of the circuit area and the number of wiring layers under the same operating frequency condition.

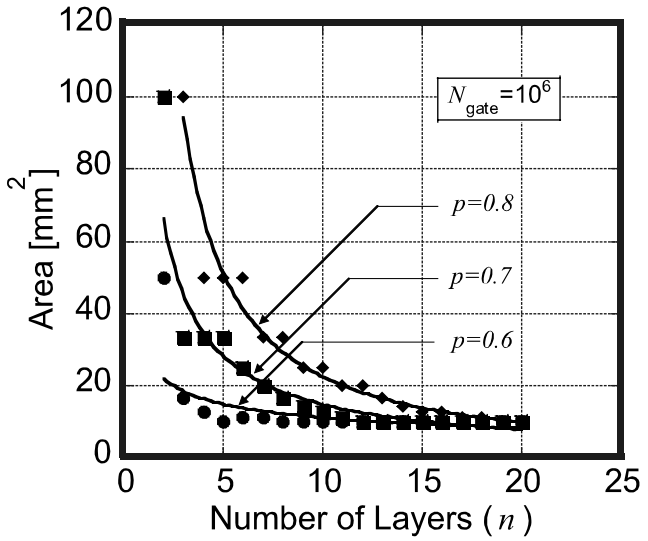


Fig.5. The relationship between circuit area and the number of layers to achieve the highest circuit operating frequency.