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Raised Source/Drain on Different Integration Schemes for Sub-micro CMOS

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1. Abstract

The performance of raised source/drain by selective epitaxial growth (SEG) using two different integration sequences is compared in this article. It was found that inserting SEG after the source/drain anneal exhibited greater benefits on reduction of junction leakage and parasitic resistance, yielding a 12% PMOS I_{on} improvement @I_{off}=10nA.

2. Introduction

As device scaling continues downward, raised source/drain provides a dual solution that reduces the junction leakage and also suppresses the short channel effect at the same time [1-2]. Moreover, SEG is able to lower the source/drain resistance by providing a sacrificial silicon layer for salicidation on fully depleted SOI and strained-Si wafers [3-4]. There are two major approaches to achieve the raised source/drain structure by selective epitaxial growth. In most reported approaches, selective epitaxy is grown before source/drain formation [5-6]. Only a few reports were found that described the insertion of selective epitaxy after source/drain formation [7]. However, inserting SEG after source/drain formation is an easier way to insert SEG into conventional CMOS processes because of its independence from source/drain profile engineering. It can also avoid the negative impact to the junction profile by the facet or defects coming from the SEG process. In this report, we evaluated these two process sequences (Fig. 1) by comparing their leakage currents, contact resistances, bridging currents, and DC performances. Furthermore, we demonstrated the improved performance of inserting SEG after source/drain anneal compared to inserting SEG directly after spacer formation.

3. Results and Discussion

Junction leakage

Figure 2(a) shows junction leakage of N+ to Pwell and P+ to Nwell. Sequence A has a similar leakage current to reference due to the comparable junction depth. However, sequence B exhibited more serious leakage compared to reference by 2 orders of magnitude (10^{-9} vs. 10^{-11}), due to the shallower junction caused by implanting through an added Si layer on the source/drain area. Similar results were observed on contact leakage current (Fig. 2(b)). By adjusting S/D and halo implant energy, the leakage current of sequence B can be lowered to the comparable level of reference (Fig. 2, case C).

Bridging

Sequence A bares a more robust non-bridging issue than sequence B. For both sequence A and B, leakage current between poly lines through field oxide is comparable to reference indicating no bridge via extension from poly tip (Fig. 3(a)). However, leakage current between poly lines through the active area shows a slightly upward trend for sequence B (Fig. 3(b)). More aggressive pre-epi wet clean before SEG worsens leakage current. From a TEM cross-section check, spacer showed serious undercut due to the HF dip before SEG. Sequence A has fewer cases of undercut because the spacer was densified in the source/drain anneal process. We believe these voids are responsible for the high leakage path. Optimized SEG process can provide a better lateral growth to occupy the hole under nitride spacer (Fig. 4) and reduce the leakage current to around 1E-7A.

Contact Resistance

Sequence A has lower N+ contact resistance than reference and sequence B (Fig. 5). A TEM cross-section check shows a white interfacial layer between contact and silicide on sequence B (Fig. 6) as well as reference wafers. EELS analysis reveals that a white layer in the interface is silicon dioxide (Fig. 7a). We believe an undoped selective epitaxy layer above the N+ area protects the electron-rich surface from oxidation in sequence A (Fig. 7b).

Device Performance

The DC performance of different sequences and reference is plotted on Fig. 8. Sequence A achieved a 12% PMOS improvement from 240μA to 270μA @I_{off}=10nA while sequence B realized a 7% PMOS improvement to 257μA @I_{off}=10nA. However, NMOS performance was degraded for both sequence A and B. The degradation of NMOS might be attributed to the source/drain deactivation by SEG thermal (Fig. 9). The tighter data variation of sequence A over sequence B confirms the better control of the source/drain profile.

4. Conclusion

We have demonstrated that selective epitaxial growth after S/D formation is a better performing and easier process sequence to insert selective epitaxial growth for forming raised source/drain implanted in 65 nm CMOS and beyond.

References

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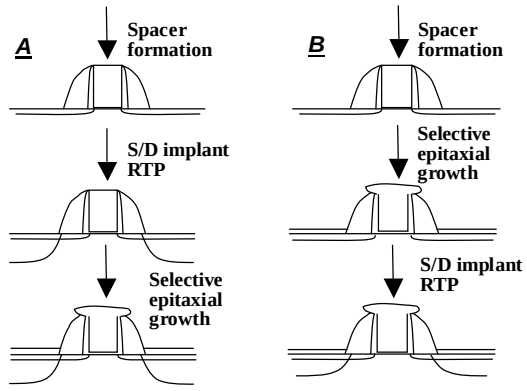

Figure 1. Different fabrication process sequences mentioned in this paper.

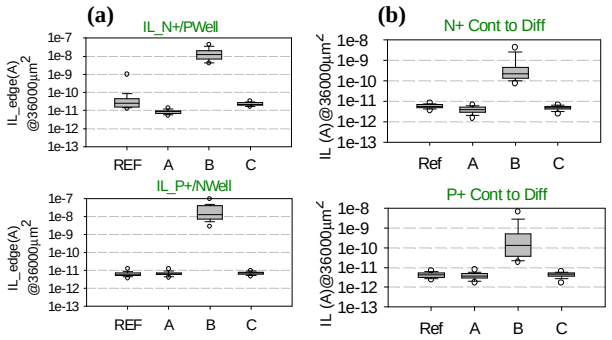

Figure 2. Junction leakage of N+/P Well and P+/N well (a) and leakage of borderless contact (b) for reference and sequence A, B, and sequence B with adjusting S/D and halo implant (C).

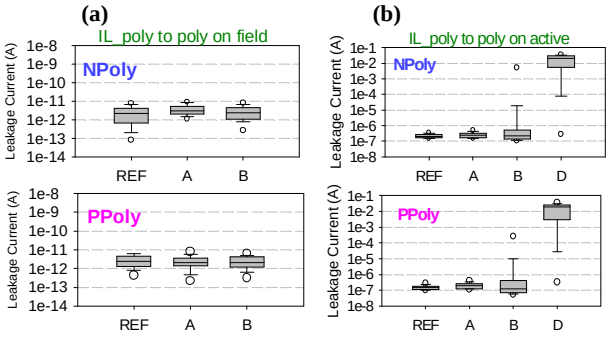

Figure 3. Leakage currents of poly to poly on field oxide (a) and poly to poly on active (b) for reference, sequence A and B. No observed leakage current was found from poly to poly on field oxide. However, more aggressive pre-epi wet clean including longer HF dipping time to achieve cleaner surface for SEG in sequence B will lead to serious leakage current (D).

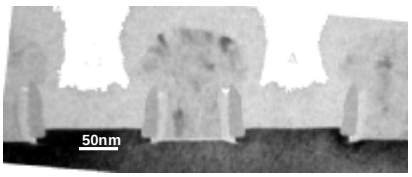

Figure 4. TEM cross-section of raised source/drain architecture for optimized SEG process in sequence B.

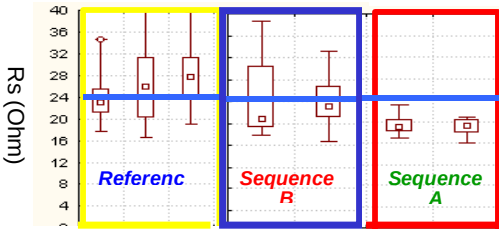

Figure 5. N+ contact resistance for reference, sequence A and sequence B.

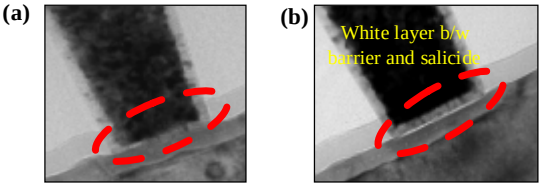

Figure 6. TEM cross-session check of N+ contact on silicide for sequence A (a) and B (b). A white layer was found between contact barrier and silicide on sequence B wafer. Reference wafer showed the same phenomena as sequence B.

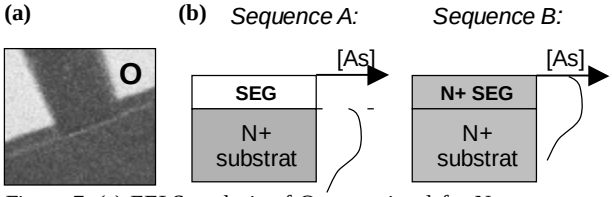

Figure 7. (a) EELS analysis of Oxygen signal for N+ contact on sequence B wafer. The white layer between contact and silicide was identified as SiO_2. (b) As concentration profile in sequence A and B.

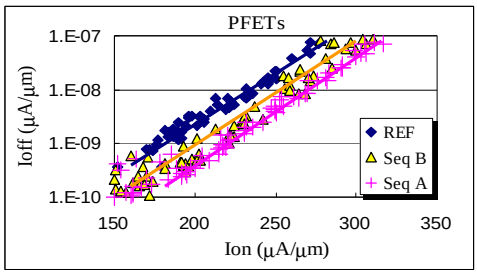

Figure 8. PFETs DC performance at 1.0V. Sequence A has a 12% improvement from 240μA to 270μA @I_{off}=10nA, while sequence B showed a 7% PMOS improvement to 257μA.

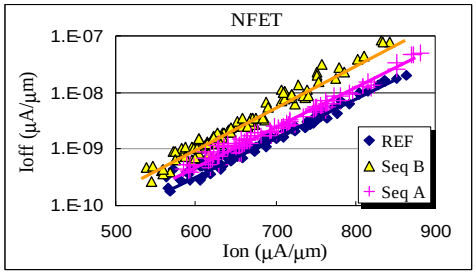

Figure 9. NFETs DC performance at 1.0V. Sequence B has the largest I_{off} at the same I_{on} than sequence A and reference.