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Design and Fabrication of MOS Device Circuits with Reticle-Free Exposure Method

Katsuhiko Wakasugi[1], Satoshi Wakimoto[1], Akira Nakada[1], Ichiro Ohshima[1], Hiroshi Kubota[1], and Kazumitsu Nakamura[2]

[1]Graduate School of Science and Technology, Kumamoto University
2-39-1 Kurokami, Kumamoto 860-8555, Japan
Phone: +81-96-342-3035 E-mail: wakasugi@st.eecs.kumamoto-u.ac.jp
[2]Kumamoto Technology and Industry Foundation
2081-10 Tabaru, Mashikimatchi, Kumamoto 861-2202, Japan

1. Introduction

In fabrication of semiconductor devices, increase in mask cost and mask turn-around-time (TAT) becomes serious problem. Furthermore, it is frequently necessary to change the design for circuit correction and additional function after the mask production. Consequently, development cost becomes high and production period becomes long. On the other hand, the market is diversified by informational globalization. In order to fill it, the product cycle must be in short-period extremely. The semiconductor manufacture industry is demanded to make large-item small- volume products with shorter TAT and lower price.

In order to solve these problems, several approaches for maskless lithography have been proposed [1]-[4]. Among them liquid crystal display (LCD) in place of the mask for the optical lithography have been demonstrated [2]-[4]. In our previous work, the method of exposure with LCD projection image and the algorithm of circuit pattern data conversion have already been reported as reticle-free exposure method [3][4]. However, actual semiconductor device fabrications by reticle-free exposure method have not been discussed.

The purpose of this paper is to verify the reticle-free exposure method being applicable to LSI manufacturing. The design and fabrication results for n-MOS transistor process with reticle-free exposure method shown in order to compare with conventional design and fabrication.

2. Reticle-free exposure method

Fig. 1 shows the configuration of the system for the reticle-free exposure method. An LCD was used in place of the conventional reticles. The light source was g-line (wavelength: 436nm). The pattern designed by CAD can be converted to bitmap format image, and displayed on the LCD. The image on the LCD is directly projected onto a wafer through the reduction lens (1/5) of a stepper. Fig. 2 shows the exposure sequence for pixel fill-in. The LCD active area is smaller than the pixel size because each section has a black matrix region. When the image displayed on the LCD is projected onto a wafer, some portion of the circuit pattern can not be exposed. This corresponds to (A-B) in Fig. 2 because of the existence of the black matrix. In order to simplify the data generation, one pixel is exposed by two steps movement for the X and Y directions to fill in the black matrix region of the pixels. This sequence is also illustrated in Fig. 2. Sequence #1 through #4 shows each step of the active area exposure, with subsequent wafer-stage step-motion. The distance of the wafer stage movement corresponds to one fifth of the exposed size of the active matrix (i.e., (A-B)/5).

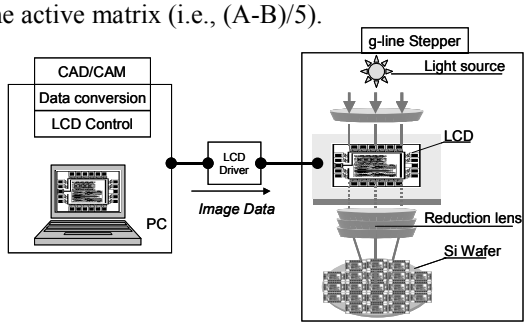

Fig. 1 LCD Reticle-Free Exposure system overview

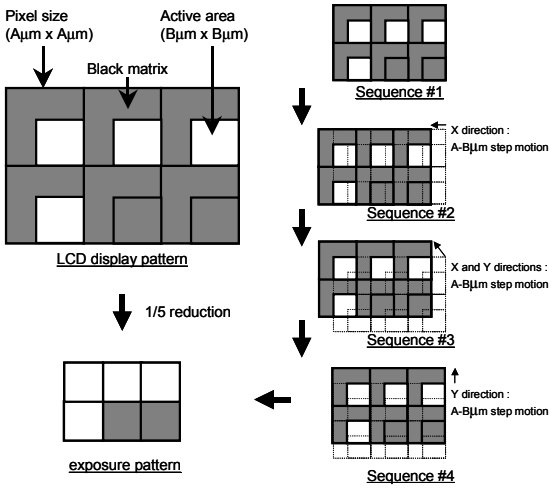

Fig. 2 Exposure sequence for pixel fill-in

3. Circuit pattern data conversion

The circuit pattern data is designed with a common CAD system. The pattern data conversion algorithm and the flow from CAD data into a bitmap format data are illustrated in Fig. 3. The structure of the circuit data is generally defined as polygons with a hierarchical structure. The first step of the conversion is to collapse the hierarchy to a

flat database and extract the polygons point coordinates data. The second step is to generate bitmap data by fitting the polygon data to their respective pixels.

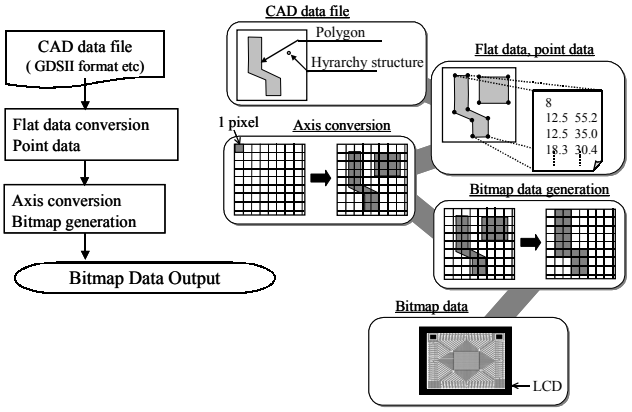

Fig. 3 Circuit pattern data conversion algorithm

4. Experiment

The fabrication of a semiconductor device was demonstrated for an n-MOS transistor process, which include four design layers. The test circuits, i.e. multiplier, ring- oscillator, test-element-groups, and so on, was designed by CAD with chip size of 5.0x3.0mm, that corresponded to the 1024x768 pixels on LCD. Alignment patterns were also put on each layer. The feature size was 5.2um that is defined by the pixel size of 26um of the LCD.

The process was following. Field oxide was formed on the 4" p-Si(100) wafer. The 1st patterning for active layer was conducted on the filed oxide. After gate oxidation, the gate material was deposited on the wafer. Then the 2nd patterning for gate was carried out. After formation of n+ source/drain, interlayer was formed on the gate pattern followed by the 3rd patterning for contact. Finally, metal interconnect was formed by the 4th patterning.

5. Results and Discussion

The comparison results of the design rule for reticle-free exposure method and general design rule (λrule) are shown in Table I. The patterning units is identical with the one fifth of LCD pixel size; a 5.2-μm square in this case. Therefore, 0.5λ patterning or sizing are impossible. As results, layout area will be larger than general design method. As one method for solving this problem, how to apply offset of 0.5λ to the center coordinates of a wafer stage at the 2nd layer exposure.

Fig. 4 shows the test device exposure results. Fig. 4 (a) shows a 4" wafer overview exposed by g-line stepper. Fig.4 (b) shows the photomicrograph of the gate after etching. The alignment mark can be automatically detected and the global alignment sequence was able to execute. Fig. 4 (c), (d) shows the photomicrograph of metarization results.

In these results, the design rule for Reticle-Free Exposure Technology has verified, and it filled global alignment accuracy.

Table I Comparison of the design rule

	λrule	Reticle-Free Design rule
1. Poly		
1.1 Minimum size	1λ	1λ
1.2 Minimum spacing	1λ	1λ
1.3 Spacing to Active	0.5λ	1λ
1.4 Gate Extension	1λ	1λ
2. Contact/Via		
2.1 Minimum size	1λ	1λ
2.2 Minimum spacing	1λ	1λ
2.5 Minimum overlap of Metal	0.5λ	1λ
3. Metal		
3.1 Minimum size	1.5λ	1λ
3.2 Minimum spacing	1.5λ	1λ

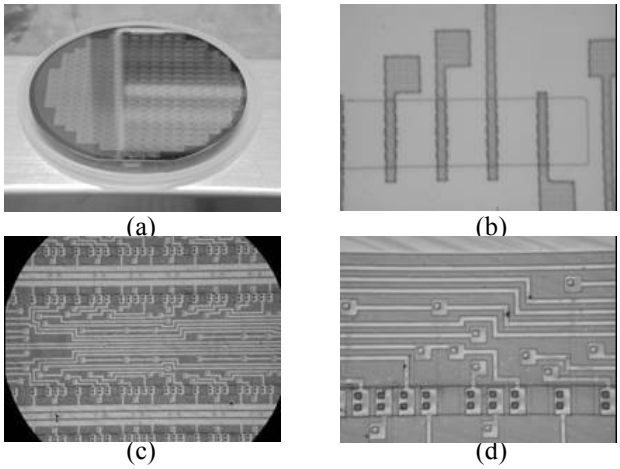

Fig. 4 Overlap exposure results of the test device.

4. Summary and Conclusions

This paper was examined the design and manufacturing of LSI which allied reticle-free exposure method. The design rule was verified, and filled the global alignment accuracy. Therefore, this LCD reticle-free exposure method has the potential of replacing conventional reticles in optical stepper lithography.

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