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Effect of Post Thermal Processes on Nitride/W/WN_x/poly-Si Gate Stack

Heung-Jae Cho, Se-Aug Jang, Yong Soo Kim, Kwan-Yong Lim, Jae-Geun Oh, Jung-Ho Lee, Tae-Su Park, Tae-Sun Back, Jun-Mo Yang, Hong-Seon Yang, Hyun-Chul Sohn, and Jin-Woong Kim
Memory R&D Division, Hynix Semiconductor Inc., Ichon P.O. Box 1010, Ichon-si, Kyoungki-do 467-701, Korea
(Phone: +82-31-630-4466, Fax: +82-31-630-4545, e-mail: heungjae.cho@hynix.com)

INTRODUCTION

As semiconductor devices are shrinking and highly integrated, mechanical stresses that occur during device fabrication have been becoming a critical issue[1~3]. In DRAM technology, tungsten (W)/polycrystalline-Si (poly-Si) gate and self-aligned contact (SAC) processes employing a thick nitride film on the W/poly-Si have been widely studied to realize improvement of the device speed and a reliable landing pad formation, respectively. Although these processes are indispensable for sub-100nm DRAM device integration, there has been no report for the effect of mechanical stress on gate oxide reliability in the nitride/W/poly-Si gate stack during thermal processes.

In this paper, we investigated the effects of the mechanical stress caused by post thermal budgets on the gate oxide reliability in the nitride/W/poly-Si gated MOS capacitor in detail.

EXPERIMENTAL

The nitride/W/WN_x/poly-Si gated MOS capacitors with shallow trench isolation were fabricated on the p-type (100) Si substrate. *In-situ* phosphorus-doped poly-Si (700Å) was deposited on the gate oxide (50Å). Furnace anneal was performed in order to activate dopants in poly-Si at 700℃. The W/WN_x (700Å) electrodes were sputter-deposited, followed by nitride deposition (3000Å) by using plasma-enhanced chemical vapor deposition (PECVD).

To evaluate the effect of post-thermal cycles on the gate oxide, we prepared several samples that received different thermal budgets after gate stack patterning as summarized in Table I.

RESULTS AND DISCUSSION

Shown in Fig. 1 show the high frequency C-V curves of MOS capacitors, exhibiting distinct differences in flat-band voltages (V_{fb}) and curve shapes with different post-thermal budgets. The samples annealed at higher temperatures display more shift of V_{fb} toward the positive direction and also more stretch-out in the depletion region. These behaviors indicate that negative charges in the gate oxide and interface states between SiO_2 and Si were generated, respectively. Figure 2 exhibits the interface trap density (D_{it}) extracted by the conductance loss method. It is clear that the interface characteristic is degraded with increasing temperatures. The S1 annealed at the lowest temperature has the D_{it} of low 10^{10} $eV^{-1}cm^{-2}$, whereas the S4 at the highest temperature shows about 1 order of magnitude higher D_{it}.

Stress-induced leakage current (SILC) and charge-to-breakdown (Q_{bd}) characteristics of MOS capacitors are shown in Fig. 3 and 4, respectively. The SILC was measured at the sensing voltage of –4.9V after electrical stressing of $-1C/cm^2$. The SILC and Q_{bd} are also observed to be degraded with increasing temperatures. It is interesting to observe that the SILC density of samples 2, 3, and 4 is dependent on the MOS capacitor area, while the S1 displays almost no area dependence. Higher SILC density is shown in the samples with larger capacitor areas, strongly implying that a mechanical stress issue is involved in these samples.

Figure 5 shows cross-sectional HRTEM images obtained from the samples 3 and 4 with the MOS capacitor area of 200 × $200um^2$. Note that nano-sized micro-voids are observed at the triple point between gate oxide and two poly-Si grains. The size of void is bigger when the post thermal budget is severer (S4 > S3). No void was observed in samples 1 and 2. These results suggest that the thermal management after gate pattering decisively affects the void formation in the nitride/W/WN_x/poly-Si gated capacitors. EDS spectra in terms of possible atomic elements conforms that there exists a real void, as shown in Fig. 5 (c) and (d). The Si concentration at the triple point (A) is lower than that at the poly-Si grain (B). The EDS analysis also rules out the possibility of segregation or contamination of other elements at the triple point.

In order to understand the electrical degradation and the micro-void formation, we investigated *in-situ* stress-temperature characteristics as shown in Fig. 6. We prepared three un-patterned wafers stacked with PECVD nitride(3000Å)/W-WN_x(700Å)/poly-Si(700Å)/SiO_2(55Å)/Si-sub. and measured the mechanical stresses by sweeping upto maximum 750℃, 800℃, and 850℃, respectively. All samples show a similar shape of hysteresis curve during heating and cooling cycles. The initial heating curves with compressive stresses change their direction to tensile state at 500~600℃. We found that the entrapped H_2 gas is abruptly released from the nitride at the almost same temperature range, as shown in Fig. 7. The PECVD nitride is well known to contain an amount of hydrogen and thermally unstable Si-H and N-H bonds[4]. Therefore, the densification of the nitride by the out-gassing is probably one of the reasons for the abrupt increase of the stress. The cooling curves exhibit no significant deviation from the tensile stress states accumulated at the maximum sweeping temperatures. A remarkable difference in the heating curves is that the higher the maximum sweeping temperature is, the more tensile stress the sample has. As a result, the hysteresis area formed by heating and cooling becomes larger when the maximum temperature is higher. It is, therefore, evident that the MOS capacitor with the PECVD nitride/W/WN_x/poly-Si gate stack experiences a severe mechanical stress during post thermal processes. The stress variations with the maximum sweeping temperatures are well consistent with both the degradation of the electrical characteristics and the micro-void size.

The micro-voids at the triple points are believed to create additional dangling and strained bonds in the oxide and at the SiO_2/Si interface, resulting in increased negative charges and interface traps. The SILC and Q_{bd} degradation are explained by the locally enhanced electric field near the micro-void during the electrical stressing due to the distorted geometry.

CONCLUSION

We observed the mechanical stress developing during post thermal processes at elevated temperatures in the nitride/W/WN_x/poly-Si structure. The thermal process induced mechanical stress was found to create nano-sized micro-voids at the triple point between gate oxide and two poly-Si grains. The micro-void is believed to cause the gate oxide degradation such as increased negative charges and interface traps and thus the SILC and Q_{bd} degradation.

REFERENCES

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TABLE I. Detailed thermal cycle sequence for each sample.

	Thermal cycle sequence
S1	450℃(H_2/N_2, 30 min)
S2	710℃(N_2, 150 min) + 450℃(H_2/N_2, 30 min)
S3	780℃(N_2, 30 min) + 450℃(H_2/N_2, 30 min)
S4	850℃(H_2/O_2, 2 min) + 710℃(N_2, 150 min) +1000℃(N_2, 10 s) + 450℃(H_2/N_2, 30 min)

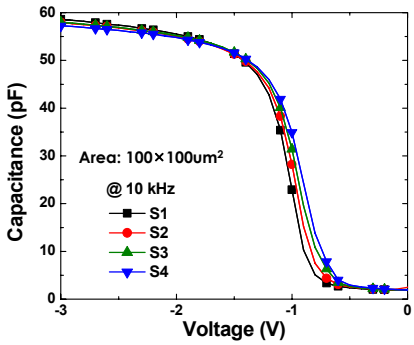

FIG. 1. High frequency (10 kHz) C-V curves of the nitride/ W/WN_x/poly-Si gated MOS capacitors with thermal budget.

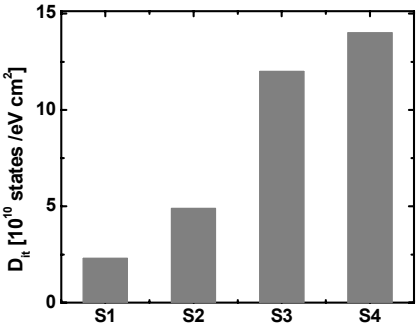

Fig. 2. Interface trap density (Dit) of each capacitor. The D_{it} was calculated from the maximum conductance loss peak by conductance method.

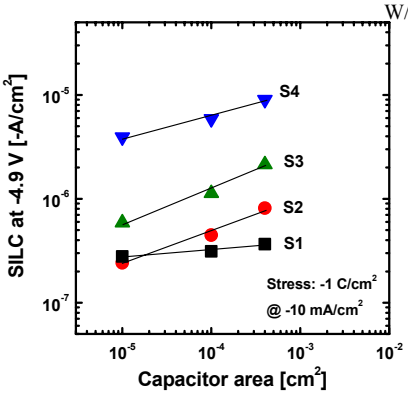

Fig. 3. Stress-induced leakage current measured on MOS capacitors with various areas. Note that the leakage current was normalized with the capacitor areas.

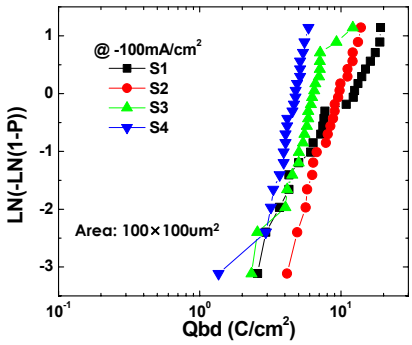

Fig. 4. Q_{bd} characteristics of MOS capacitors with thermal budget.

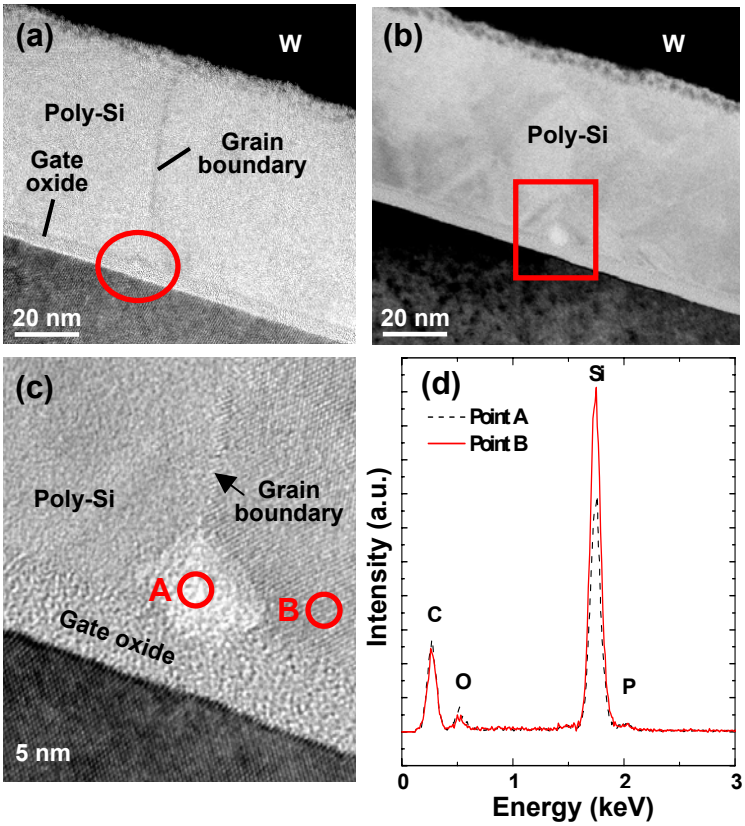

Fig. 5 . High-resolution TEM images obtained from (a) S3 and (b) S4 capacitors. The magnified image near the micro-void in Fig. 5 (b) is shown in Fig. 5 (c), whereas EDS spectra obtained from the areas of point A and B in Fig 5 (c) are displayed in Fig. 5 (d).

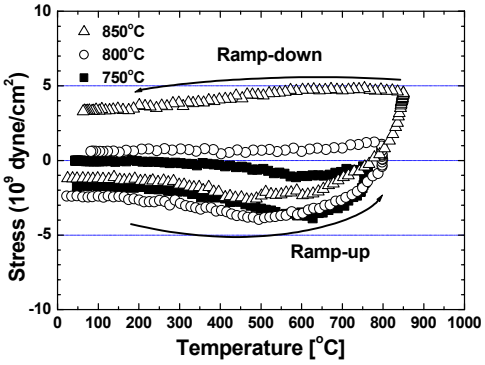

Fig. 6. *In-situ* stress curves of 8-inch wafers with the nitride/W/WN_x/poly-Si/SiO_2 stack. Three blanked wafers were prepared for sweeping up to maximum 750, 800, and 850℃, respectively.

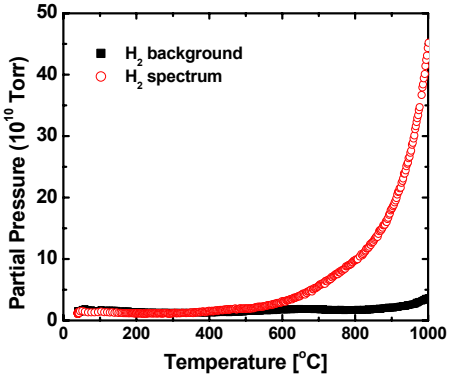

Fig. 7 . H_2 thermal desorption spectrum from nitride film measured by TDS. The background represents the desorption of H_2 from TDS apparatus.