Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 484-485

P3-20

Impact of Metal Gate/High-k Interface in Mo Metal Gated MOSFETs with HfO_2 Gate Dielectrics

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1. Introduction

As MOS devices are aggressively scaled down, the scaling of SiO_2 gate dielectrics with poly-Si gate becomes serious problem. Recently, the development of high-k dielectrics and metal gates are making rapid progress to overcome the problem. Figure 1 shows main process integration issues of metal-gated devices, that is adjustable dual work function, etching the dual metal gates, reactions with gate dielectrics during thermal process, and so on. Mo is well known as a metal of adjustable work function by using N implantation into it [1]. HfO_2 is one of the most intensively studied high-k materials [2, 3]. Therefore, we investigated and demonstrated the issues on Mo(N)/HfO_2 gate stack, focusing on the relation between Mo(N)/HfO_2 interface and electrical characteristics.

2. Experimental

Figure 2 shows process flow of the fabricated MOSFETs with Mo(N)/HfO_2 gate stack. In some devices, we used Mo(N) gate with SiO_2 gate dielectrics. N_2^+ ion was implanted into Mo to change its work function. The phenomena caused in Mo(N)/HfO_2 gate stack were analyzed using SIMS or AES. We simulated N diffusion using SUPREM4 process simulator. Mo and HfO_2 were deposited by sputtering and metal-organic chemical vapor deposition, respectively.

3. Results and Discussion

Gate etching

When Mo gate is etched, it is needed to have high etching selectivity against HfO_2 and is desirable to have the same etching rate in metals for NMOS and PMOS. In Mo and Mo(N) case, we can use the same etching rate by changing the applied RF power (Figure 3a), and obtain high selectivity to HfO_2 by increase of etching pressure (Figure 3b). Therefore, if multi-step method is applied, we can ideally etch Mo(N)/HfO_2 gate stack.

Work function

When Mo work function is changed by introducing N, N concentration near the HfO_2 interface is important. We found that N diffusion in Mo was fast below $5x10^{20}$ cm^{-3} of N concentration, and was slow at the higher concentrations (Figure 4). We extracted the slower N diffusivity at the high concentrations (Figure 5). The faster N diffusivity at the low concentrations was over 10^{-11} cm^2/s. By using these diffusivities, we calculated N concentrations near gate oxide in various annealing conditions (Figure 6). We also plotted in Fig. 6 V_{FB}s of Mo(N) gated MOS diodes fabricated using some of the annealing conditions. The V_{FB}s are well corresponding to the variation of calculated N concentrations. The maximum V_{FB} shift in this experiment was 0.7V (Figure 7). If we increase the dose of N_2 implantation, the shift is deduced to be over 0.8V. Considering a negative shift of V_{FB} that HfO_2 has, the work function of Mo(N) system can extensively cover the energy region of Si bandgap.

Reaction of Mo with HfO_2

Reaction of metal with gate oxide including oxygen extraction from gate dielectrics is serious problem to develop metal-gated MOS devices. We investigated reaction of Mo with HfO_2 using AES. When annealing time was 10 min, the reaction was observed over 850°C (Figure 8). We extracted reaction rates from these experimental data (Figure 9). We found that the rates are high even at low temperatures. Lower region in Figure10 indicates conditions for Mo not to react with HfO_2 calculating from the extracted reaction rate. In relation with this reaction limit, we also entered in Fig.10 gate leak currents of Mo gated MOS diodes. The leakage current annealed at 800°C for 2 min, which is above the reaction limit, was six orders larger than that below the limit.

Process windows

We next discuss the process windows from N diffusion and the reaction with HfO_2. Upper region in Fig. 10 indicates N diffusion conditions enough to be high N concentration, when Mo thickness is 10 nm. Apparently, there is no process window to fabricate Mo/HfO_2 gate stack from view of the reaction and N diffusion. When Mo thickness is 5 nm to be short diffusion length, however, there is still no process window. A method to suppress the reaction was SiN insertion between Mo and HfO_2 as shown in Figure 11. Therefore, we were able to create process windows by the SiN insertion and fabricate 70-nm gate-length CMOS devices with Mo(N)/HfO_2 gate stack (Figure 12).

4. Conclusions

We investigated Mo(N)/HfO_2 gate stack. We can etch Mo(N)/HfO_2 gate stack. The work function of Mo(N)/HfO_2 system can extensively cover the energy of Si bandgap. In addition, we show the issue on thermal budget from N diffusion in Mo and reaction of Mo with HfO_2. We show that SiN insertion and thinning of Mo thickness can make process windows. In this way, we fabricated 70-nm gate-length CMOS devices.

References

[1] R. Lin, et al., IEEE Electron Device Letters **23**, 49 (2002).
[2] L. Kang, et al., 2000 Symposium on VLSI Technology, p 44.
[3] Y. Morisaki, et al.,, IEDM 2002 Technical Digest, p 861.

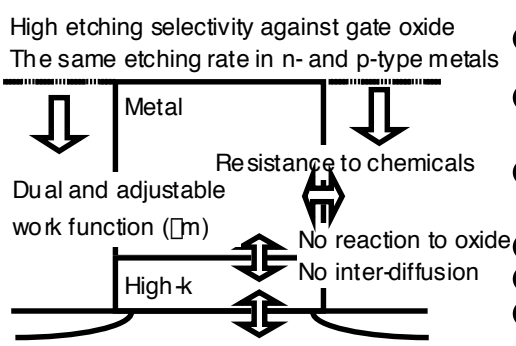

Fig.1 Schmatic drowing of process integration issues in metal/High-k gate stack

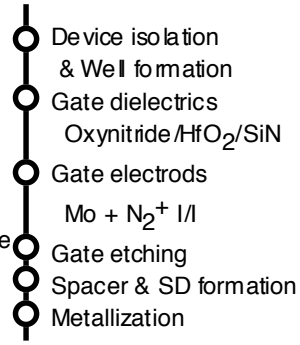

Fig. 2 Process flow of Mo metal gated MOSFETs

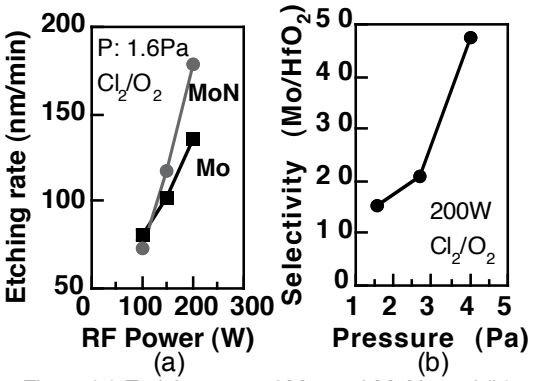

Fig. 3 (a) Etching rate of Mo and MoN, and (b) selectivity agenst HfO_2 dielectrics

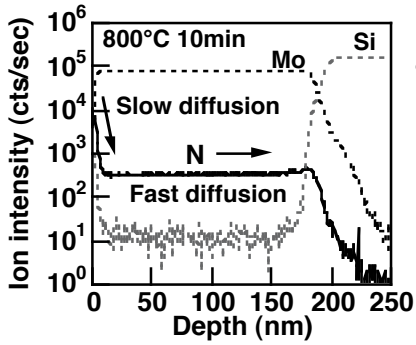

Fig. 4 N profile in Mo measered by SIMS

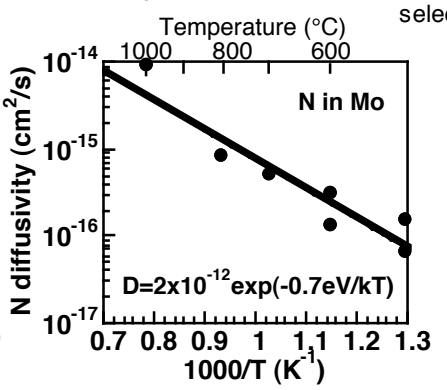

Fig.5 Extracted N diffusivity in Mo at high N concentration

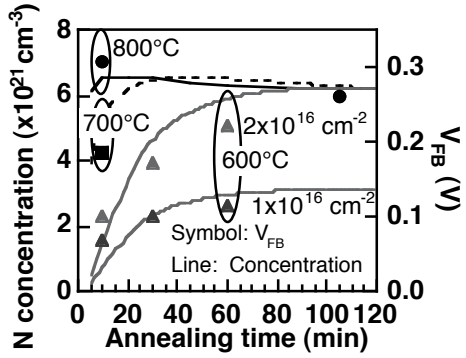

Fig.6 N concentraion calculated from the N diffusivity and V_{FB} of MOS diodes

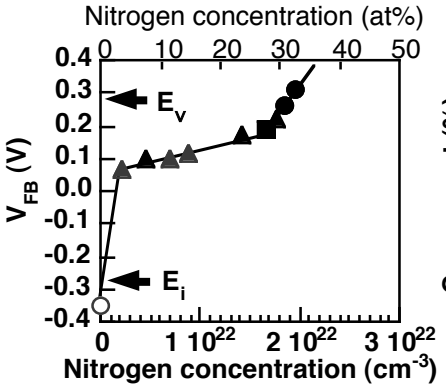

Fig.7 Relation between V_{FB} of MOS diodes and N concentration

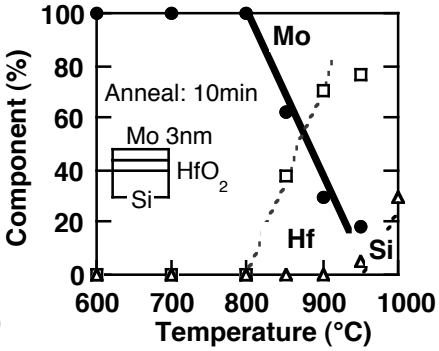

Fig.8 Reaction of Mo with HfO_2 measured by AES

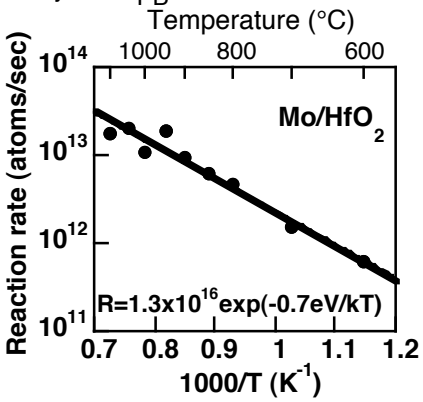

Fig.9 Mo reaction rate with HfO_2 extracted from AES data

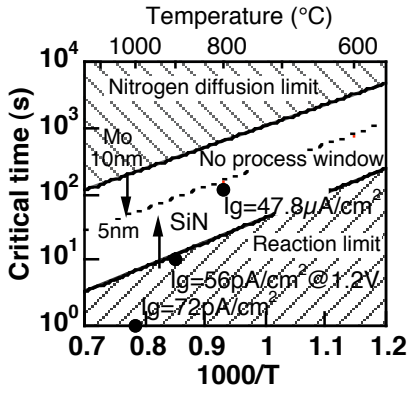

Fig.10 Process window considering from N diffusion and the reaction with HfO_2

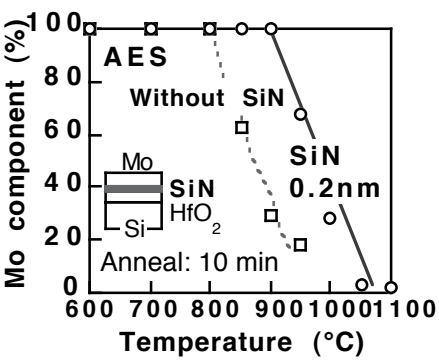

Fig.11 Suppression of the reaction by SiN insertion at Mo/HfO_2 interface

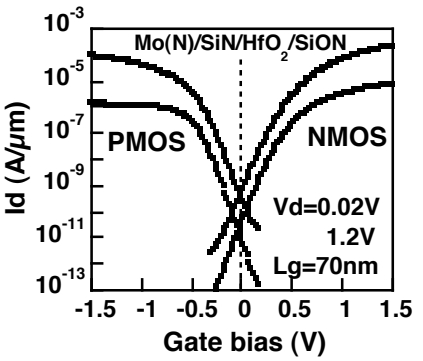

Fig.12 Id-Vg characteristics of Mo gated MOSFETs.