Flat-band Voltage Tunability and No Depletion Effect of Poly-Si Gate CMOS with Nanometer-size Metal Dots at the Poly-Si/Dielectric Interface

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1. Introduction

The conventional poly-Si gates have a serious problem of the depletion effect which increases the capacitance equivalent thickness (CET) in the inversion condition. This also significantly reduces advantages of using high-k dielectric film as a gate insulator. Therefore, introducing metal gates for advanced CMOS is strongly required. However, a big issue of metal gate is that it is hard to appropriately control the flat-band voltage, V_{FB} (or threshold voltage, V_{th}) of MOSFETs under the realistic processing conditions. In this paper, we demonstrate a new scheme for achieving V_{FB} tunability, no depletion effect and no mobility degradation in the conventional poly-Si gate process for n and pMOSFETs by introducing TaN dots at the poly-Si/SiO₂ interface.

2. Experimental

The MOSFET fabrication process flow is summarized in **Fig. 1**. After the conventional LOCOS isolation, various thicknesses of TaN films were deposited on 4 nm-thick thermally grown SiO₂ by using the MOCVD process [1]. Then, 150 nm-thick undoped amorphous Si was deposited on the ultra-thin TaN at 525°C. After the gate patterning, P or BF₂ of $3x10^{15}$ cm⁻² was implanted at 30 keV or 35keV, respectively, followed by 200 nm-thick SiO₂ deposition. The activation annealing was carried out at 950°C in N₂ ambient for 20 s, as in the case of the conventional CMOS fabrication process.

3. Results and Discussion

Figure 2 shows a cross-sectional TEM image, a schematic illustration and a SIMS profile of n^+ poly-Si/TaN /SiO₂/Si structure after the MOSFET fabrication. It is shown that the deposited TaN forms a dot structure rather than a uniform thin film for the case of 0.5-nm TaN deposition. The dot diameter is roughly 2nm. It is likely that the TaN dot formation is due to the thin film agglomeration phenomena. Furthermore, it is noted that the diameter and the density of TaN dots are increased with TaN thickness up to 5 nm. The SIMS profile shows that both Ta and N atoms exist only in the poly-Si/SiO₂ interface.

Figure 3 shows the high frequency C-V characteristics of nMOSFETs from the accumulation to the inversion. It is clearly shown that the V_{FB} (and V_{th}) shifts from the ideal value corresponding to the case with 0nm thick TaN (simple poly-Si gate) to the positive direction by 0.6 V with increasing the TaN thickness on SiO₂. This fact means that the effective work function on SiO₂ can be varied from the conduction band edge to the midgap of Si in nMOSFETs,

while from the valence band edge to the midgap in pMOSFETs. It has been reported that in the thick TaN case the effective work function of TaN electrode approaches the midgap after a high temperature process [1]. Thus, it is expected that the effective work function changes from the n^+ poly-Si (or p^+ poly-Si) level towards the midgap region by increasing the TaN thickness. **Figure 4** shows a schematic band diagram in which a range of the effective work function tuned by introducing the TaN dot layer at the poly-Si gate/SiO₂ interface is indicated. Thus, it can be concluded that the effective work functions are tunable by changing the TaN thickness within 1nm.

Another big concern in poly-Si gate CMOS is the poly-Si depletion effect. Figure 3 shows that a significant poly-Si depletion effect is observed in the case of no TaN deposition, while almost a comparable saturated capacitance for both accumulation and inversion is obtained in the case of 0.5 nm TaN deposition. Furthermore, in Fig. 3 we note that the saturated capacitance value at a fixed V_g depends on the deposited TaN thickness. This fact indicates that the inversion and accumulation CETs increase with increasing the TaN thickness, though the detailed mechanism remains unknown.

Figure 5 shows CET in the inversion region and V_{FB} shifts from the control devices for n and pMOSFETs as a function of the deposited TaN thickness. The positive and negative V_{FB} shifts mean the difference from the V_{FB} of n⁺ and p⁺ poly-Si gate, respectively. From those results, appropriate V_{FB} can be tuned at the expense of a small depletion effect of poly-Si gates for TaN layer thinner than 1nm.

Figure 6 shows electron and hole mobility characteristics of n and pMOSFETs with TaN dots of 0.5 and 1.0 nm thickness at the poly-Si/SiO₂ interface. Though it has been reported [2] that the inversion layer mobility of nMOSFETs with thicker W gate electrode was degraded, no mobility degradation is observed in the case of forming TaN dots at the poly-Si gate/SiO₂ interface, as compared with the results of conventional n^+ poly-Si and p^+ poly-Si gates.

4. Conclusions

We have investigated a new gate stack structure with nanometer size metal (TaN) dots at the poly-Si/SiO₂ interface. In the new structure, V_{FB} can be tuned over the wide range for nMOSFET as well as for pMOSFET. Furthermore, the poly-Si depletion effect is effectively suppressed without the mobility degradation. This gate stack structure is fully compatible with the conventional poly-Si gate process, and could be a promising gate electrode formation process for the advanced metal gate CMOS.

Acknowledgements

This work was supported by NEDO. References

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Fig. 1. MOSFET fabrication process flow for a new gate structure with TaN dots on SiO₂. It is fully compatible with the conventional poly-Si gate process.



Fig. 3. High frequency C-V curves measured for nMOSFETs (L/W= $100\mu m / 100\mu m$) from accumulation to inversion. Almost comparable saturated capacitance values for both accumulation and inversion are successfully obtained even in the case of TaN dots with 0.5 nm thickness.



Fig. 5. The inversion CET and V_{FB} shift measured as a function of TaN thickness for n and pMOSFETs. The effective work function on SiO₂ can be varied from that of n⁺ poly-Si to the midgap of Si, and from that of p⁺ poly-Si to the midgap. Appropriate V_{FB} values can be selected at the expense of a very small CET increase due to the poly-Si depletion effect.

n+

poly-S

SiO

Si

(b) SIMS profile of the gate stack



Fig. 2. (a) Cross-sectional TEM image, schematic illustration of the gate stack with TaN dots and (b) SIMS profile of the gate stack for 0.5 nm-thick TaN deposition on SiO₂. Metal dots with roughly 2 nm diameter at the n^+ poly-Si/SiO₂ interface are clearly observed instead of an ultra-thin uniform TaN film. The SIMS profile shows that both Ta and N atoms exist only in the poly-Si/SiO₂ interface.







