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Workfunction Tuning Using Various Impurities for Fully Silicided NiSi Gate

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1. Introduction

Metal gates are expected to replace poly-Si gates that accompany a depletion effect problem. For the purpose metal workfunction tuning must be accomplished maintaining compatibility to conventional CMOS fabrication process. Fully silicided NiSi is expected to satisfy these requirments [1-3]. The workfunction of intrinsic NiSi locates near midgap of Si. The NiSi workfunction is changed by impurity pileup formed at the oxide interface. Impurities in poly-Si are swept out by the silicidation ("snowplow effect" [4]) [1] and the pileup is formed by the silicidation, as illustrated in Fig. 1. It is considered that the workfunction can be shifted if impurities at the oxide interface form high density dipoles [5], as shown in Fig. 2. However, as shown in Fig. 3, the NiSi workfunction shift reported to date using P, As, Sb, and B [1, 2] is insufficient. We have investigated how to enlarge the NiSi workfunction tunable range changing impurities and silicidation conditions.

2. Experiments

Fully silicided NiSi gate MOS diodes were fabricated as follows. Starting with p-Si substrates, LOCOS formation, gate oxidation, gate poly-Si deposition were carried out, in turn. Thicknesses for the gate oxide and gate poly-Si were 10 nm and 100 nm, respectively. Then, impurities (N, F, Sb, As, P, B, Ge, or In) were implanted into the poly-Si gate. After gate patterning, the gate was fully silicided utilizing in-situ lamp heating in the vacuum, just after 60 nm Ni sputter deposition. Silicidation temperature was 400°C, 450°C, or 500°C. Finally the unreacted Ni removal and PMA (Post Metallization Anneal) were carried out to complete the MOS diode fabrication.

3. Results and Discussion

Table 1 shows brief summary of ΔV_{FB} for various impurities. C-V characteristics of the MOS diodes with Sb, As, P, B, and Ge showed flat-band voltage shift, and those with N and F resulted in no shift. It is noteworthy that Ge that is not a dopant for Si gave rise to V_{FB} shift. This implies that the NiSi workfunction could be tuned more widely with impurities other than dopants. In the case of In, the complicated changes including decrease in accumulation capacitance were observed.

Firstly, detailed experimental results with Sb are described. Sb depth profiles after the full silicidation for the various silicidation temperatures are shown in Fig. 4. The Sb pileup at the oxide interface for 400°C is larger than for 500°C. Sb peak formed by the implantation vasnishes at 400°C. Lower silicidation temperature that leads to lower silicidation rate seems to increase swept-out impurities by the snowplow effect and the pileup. Figure 5 shows C-V characteristics for MOS diodes with Sb. Though silicidation at 500°C results in small ΔV_{FB}, it was increased by reducing the temperature. At the same time, ΔV_{FB} increase seems to saturate against the temprature under 400°C. If the dipole density is proportional to Sb concentration at the interface, ΔV_{FB} is also proportional to it. However, pileup growth results in impurity precipitation at the interface in the end. In truth, partial film peeling was found after unreacted Ni removal with acid only for specimens silicided at 400°C. This is probably attributable to the Sb precipitation at the interface and may be the origin of ΔV_{FB} shift saturation. Improvement of ΔV_{FB} using Ge was also attempted in the same manner as the case with Sb. Variation in Ge depth profiles by Ge dose change is shown in Fig. 6. Ge concentration at the oxide interface increased by increasing the Ge dose from $5x10^{15}$ cm^{-2} to $1x10^{16}$ cm^{-2}. However, both Ge dose increase and silicidation temperature lowering were not effective to increase ΔV_{FB}, as shown in Fig. 7. The relationship between these results and Ge precipitation formation is not clear to date.

Figure 8 shows the complicated changes in C-V characteristics, for the diodes fabricated with In. Decrease in accumulation capacitance and the V_{FB} shift are observed, as shown in Fig. 8(a). Since insulator film formation that accompanies charge formation was suspected, SiN was deposited on the oxide to prevent interfacial reaction. In this case, ΔV_{FB} tunned to be negligibly small, as shown in Fig. 8(b). Though mechanisms of these changes are not clear yet, the results should be noted as one of the roadblocks against practical use of NiSi as a gate material.

4. Conclusion

Flatband voltage shift of NiSi gate MOS diodes were investigated with predoping and full silicidation technique. It was found that silicidation temperature is an important key factor to enhance the snowplow effect and enlarge the workfunction shift. However, problems such as the precipitation at the oxide interface and interface reaction should be cleared to obtain practicaly large workfunction shift.

Acknowledgements

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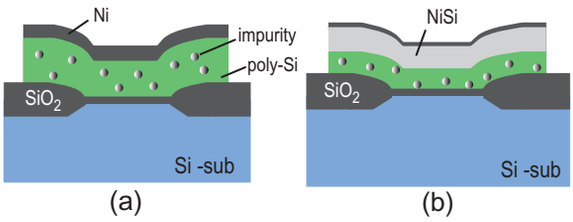
References

[1] J. Kedzierski et al., IEDM 2002. Tech. Dig. p. 247.
[2] J. Kedzierski et al., IEDM 2003. Tech. Dig. p. 315.
[3] W. P.Maszara et al., IEDM 2002. Tech. Dig. p. 367.
[4] I. Ohdomari et al., J. Appl. Phys. **56**, p. 2725 (1984).
[5] M. Hino et al., SSDM 2003. Ext. Abs. p. 494.



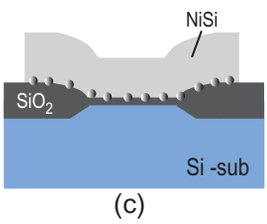


Fig.1 Model illustrations to explain pileup formation by the snowplow effect in NiSi full silicided gate. (a) before silicidation, (b) halfway and (c) after full silicidation.

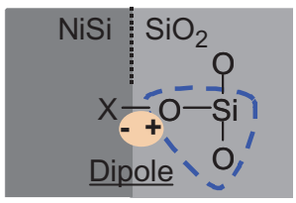


Fig.2 Electric dipole model to explain workfunction shift at the NiSi/SiO_2 interface. X stands for impurity atoms that compose the pileup.

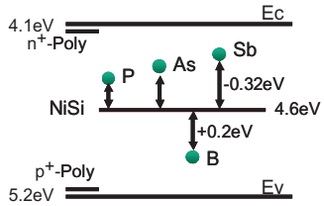


Fig.3 NiSi workfunction tunable range. Drawn based on the reports by J. Kedzierski et al. [1, 2].

Table.1 Impurity implantation conditions and V_{FB} shift.

	Dose[cm^{-2}]	Energy[KeV]	ΔV_{FB}
N	5.0 x 10^{15}	10	No
F	2.5 x 10^{15}	10	No
B	1.0 x 10^{15}	5	Yes
P	5.0 x 10^{15}	15	Yes
Sb	5.0 x 10^{15}	30	Yes
Ge	5.0 x 10^{15}	30	Yes
In	5.0 x 10^{15}	30	Yes?

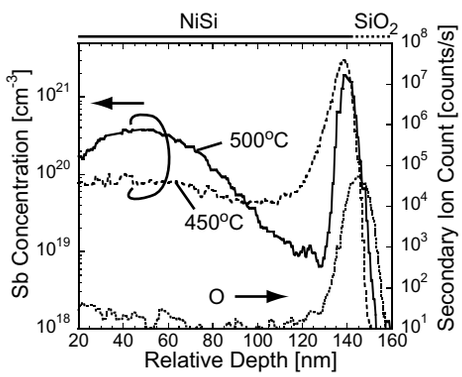


Fig.4 Sb depth profiles obtained by back-side SIMS technique. Snowplow effect was promoted by silicidation temperature lowering that lead to pileup peak concentration increase.

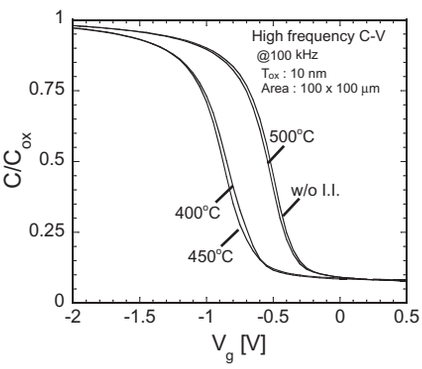


Fig.5 C-V characteristics of NiSi gate diodes with Sb. V_{FB} shift changes according to silicidation temperature.

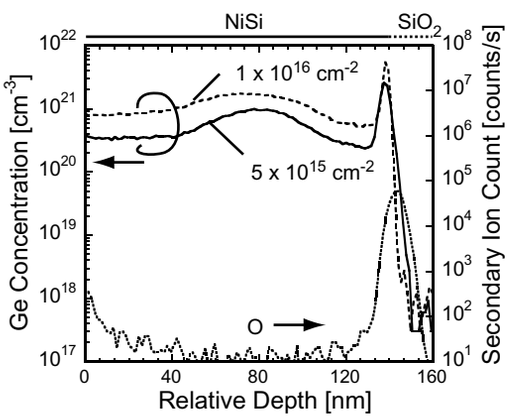
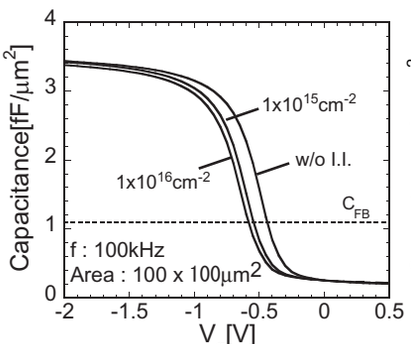


Fig.6 Ge depth profiles obtained by back-side SIMS technique. Amount of Ge pileup was increased by increasing the Ge implantation dose.



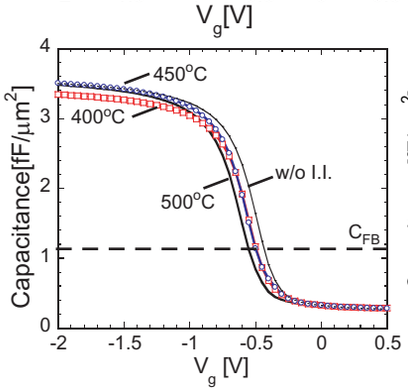
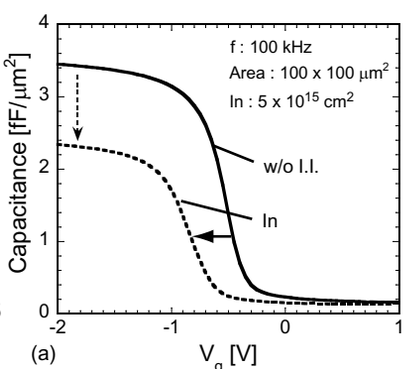


Fig.7 C-V characteristics of NiSi : Ge gate diodes. V_{FB} shift did not clearly depend on full silicidation temperature and Ge dose.



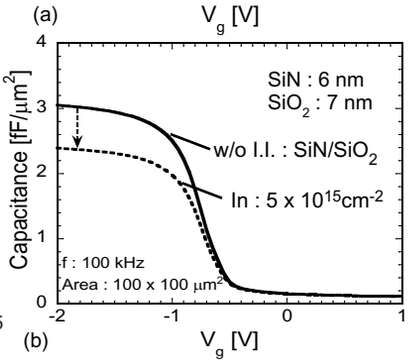


Fig.8 C-V characteristics of NiSi : In gate diodes. Gate insulator were (a)SiO_2 (b)SiN/SiO_2. SiN was deposited on SiO_2 to prevent interfacial reaction.